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L3MATRIX

LARGE, LOW POWER AND LOW COST DATA CENTRES

Research and Innovation action
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D7.3 – Project First Newsletter

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Abstract: The first L3matrix Newsletter has been produced and distributed to the OFC 2017 attendees which took place between the 19th and 23rd of March 2017 in Los Angeles, USA

Keywords: Newsletter

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PU = Public ; PP = Restricted to other programme participants (including the Commission Services) ; RE = Restricted to a group specified by the consortium (including the Commission Services) ; CO = Confidential, only for members of the consortium (including the Commission Services)

Project Information

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1 Executive Summary

The first L3matrix Newsletter was published on the 16.03.2017. The Newsletter was sent to the subscribers of the newsletter and to all the L3matrix Partners. In addition it was circulated among the attendees of the OFC 2017 conference which was organized between the 19th and 23rd of March 2017 in Los Angeles, USA

The first L3matrix Newsletter gives an overview over the project itself, its content, its mission and its objectives. Furthermore the L3matrix Partners are presented.

2 Introduction

The objective of this deliverable D7.3 is to report on the first L3matrix Newsletter.

2.1 Document structure

The present deliverable D7.3 is split into four major chapters:

- Executive summary
- Introduction
- L3matrix Newsletter Nr.1 brief description
- L3matrix Newsletter Nr.1

2.2 Audience

This document is public.

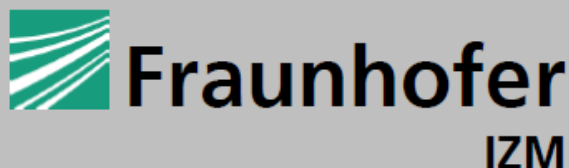
3 L3matrix Newsletter Nr.1

The first L3matrix Newsletter has been produced and distributed through different channels, electronically through the Internet and email lists to a more general audience. The document is available on our project website l3matrix.eu.

The Newsletter includes in the first edition following sections:

- Brief overview over the project and it's mission
- The project approach for a novel SiPh switching matrix
- The project objectives
- The innovation challenges we will deal with within the project
- The project final demonstrator packaging concept
- The consortium partners

Appendix L3matrix Newsletter number 1



FRAUNHOFER-INSTITUT FÜR ZUVERLÄSSIGKEIT UND MIKROINTEGRATION IZM



L3MATRIX – large, low power and low cost data centers

Concurrently, disaggregation and virtualization trends in the DC are forcing the traffic to be between servers and storage elements in the east-west direction. These changes require massive switching capabilities from the discrete switch elements. However, the technology is rapidly reaching a limit. The result is a multi-layered DC topology with high power consumption and long latency. The L3MATRIX project provides novel technological innovations in the fields of silicon photonics (SiP) and 3D device integration. The project will develop a novel SiP matrix with a scale larger than any similar device with more than 100 modulators on a single chip and will integrate embedded laser sources with a logic chip thus breaking the limitations on the bandwidth-distance product.

A novel approach will be used with embedded III-V sources on the SOI substrate which will eliminate the need to use an external light source for the modulators.

L3MATRIX provides a new method of building switching elements that are both high radix and have an extended bandwidth of 25 Gb/s in single mode fibres and waveguides with low latency. The power consumption of DC networks built with these devices is 10-fold lower compared to the conventional technology. The outcome of this approach is that large networks, in the Pb/s scale can be built as a single stage, non-blocking network.

• Dr. Tolga Tekin

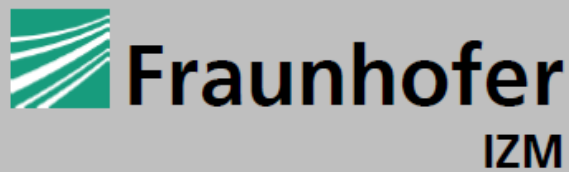
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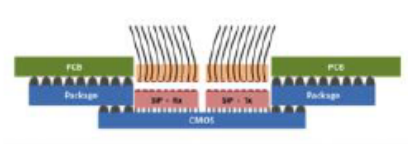


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FRAUNHOFER-INSTITUT FÜR ZUVERLÄSSIGKEIT UND MIKROINTEGRATION IZM

L3MATRIX – large, low power and low cost data centers



Objectives, potential technology breakthroughs, specific innovation challenges and potential market barriers:

- Scaling of the network to provide a solution to the growing demands for bandwidth.
- Increasing the reach of the optical interconnects within the site given its size and the need to connect servers directly in the east-west direction
- Minimizing the port-to-port latency to enable timing-critical processes such as disaggregated memory access or cache-coherent systems.
- Cost reduction, primarily in electrical power consumption and total cost of ownership.
- Two-dimensional Silicon Photonics chip with 128 lanes on 100mm² requiring a density of ~0.8mm² per channel including integrated hybrid silicon III-V laser sources

- Improvement of the power efficiency to the 3pJ/bit range
- Reduce the port-to-port latency to less than 20ns
- Scalable data centre architecture into the Pb/s scale

Partners:

- FRAUNHOFER IZM | Germany
- DUST Photonics | Israel
- AMS AG | Austria
- IBM RESEARCH GMBH | Switzerland
- ARISTOTELIO PANEPISTIMIO THESSALONIKIS | Greece
- UNIVERSITAT POLITECNICA DE VALENCIA | Spain
- BRIGHT PHOTONICS BV | Netherlands
- UNIVERSITY COLLEGE LONDON | United Kingdom