Chip and system-level integration technologies for silicon photonics

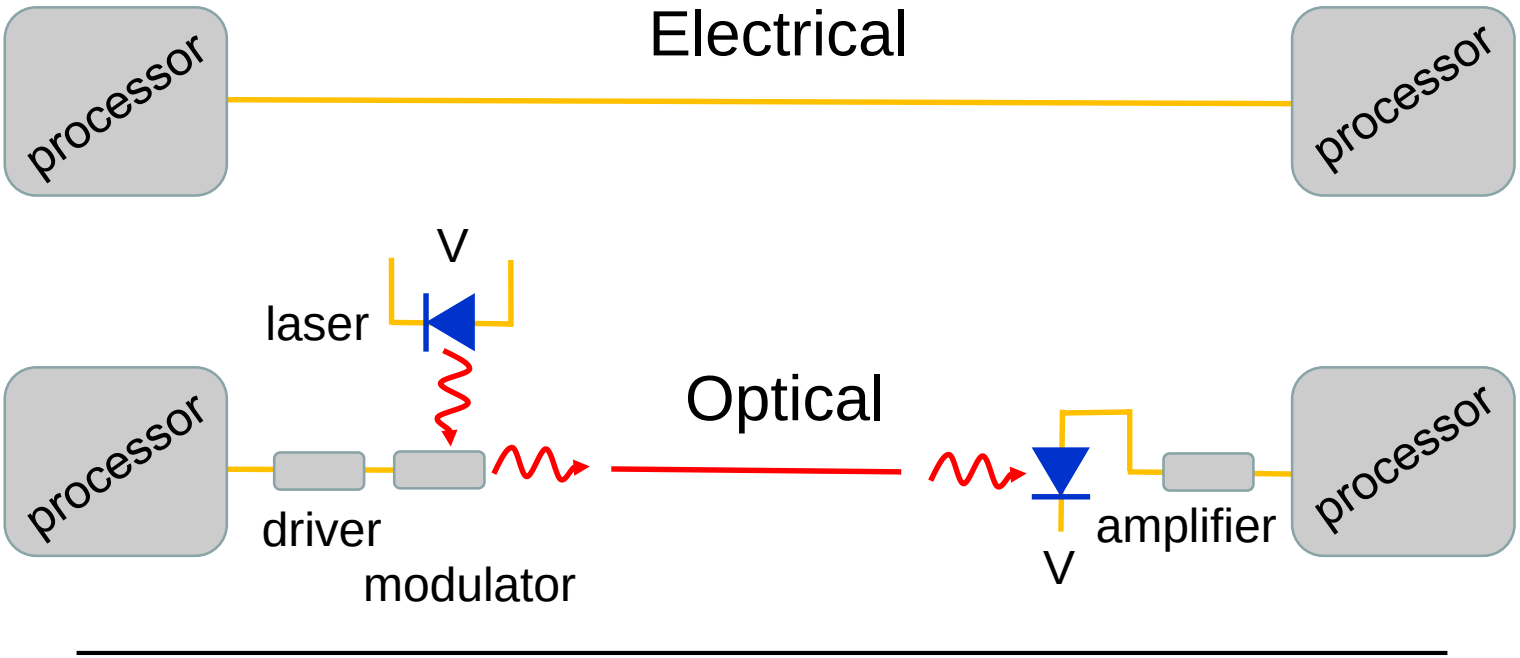
Bert Jan Offrein

5th International Symposium for Optical Interconnect in Data Centres

Outline

- The need for integration at component and system level
  - CMOS silicon photonics with embedded III-V materials
  - High channel count silicon photonics packaging
- Summary

Communication between two processors



Optical communication:

- 1000 x Larger bandwidth
- 1000 x Lower loss
- 100 x Larger distance

Scalability & Power efficiency !!!

Optical communication requires many more components and assembly steps !!!

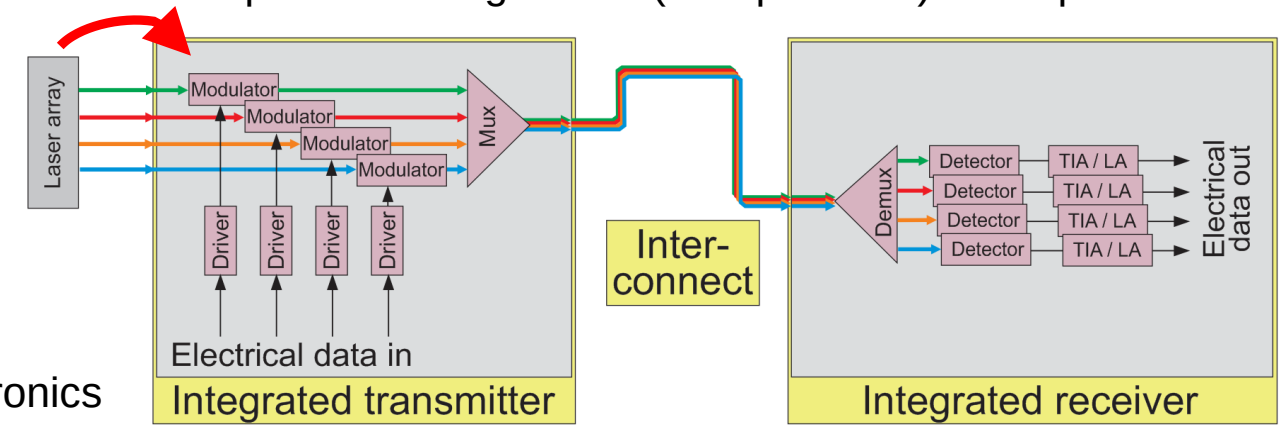
Photonics technologies for system-level integration

1 Chip-level: CMOS silicon photonics + Active photonics devices

- Si photonics provides all required buliding blocks (except lasers) on chip-level:

  - Modulators
  - Drivers
  - Detectors
  - Amplifiers
  - WDM filters

  + CMOS electronics



2 System-level: Scalable chip-to-fiber connectivity

- One step mating of numerous optical interfaces
- Provide electrical and optical signal routing capability
- Enable a simultaneous interfacing of electrical and optical connections

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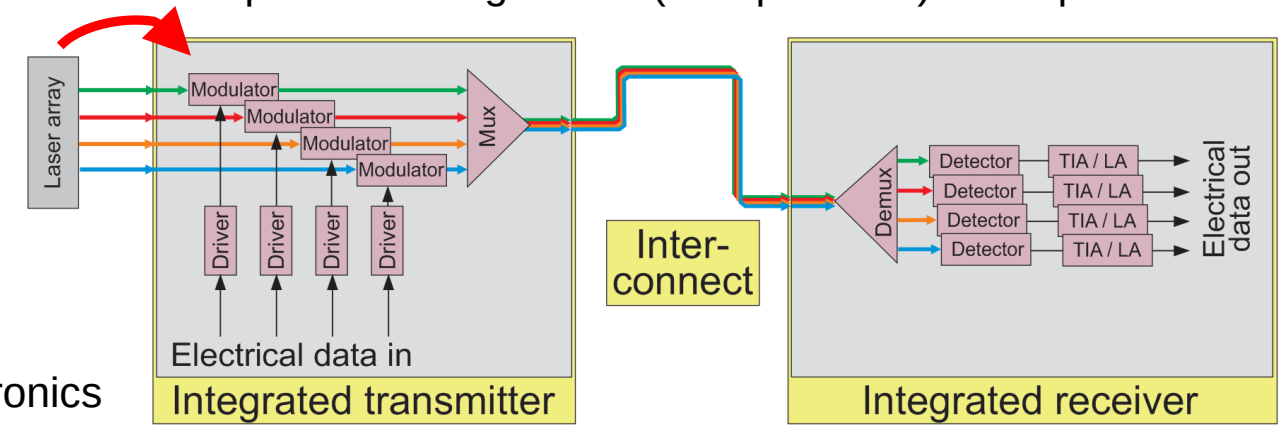

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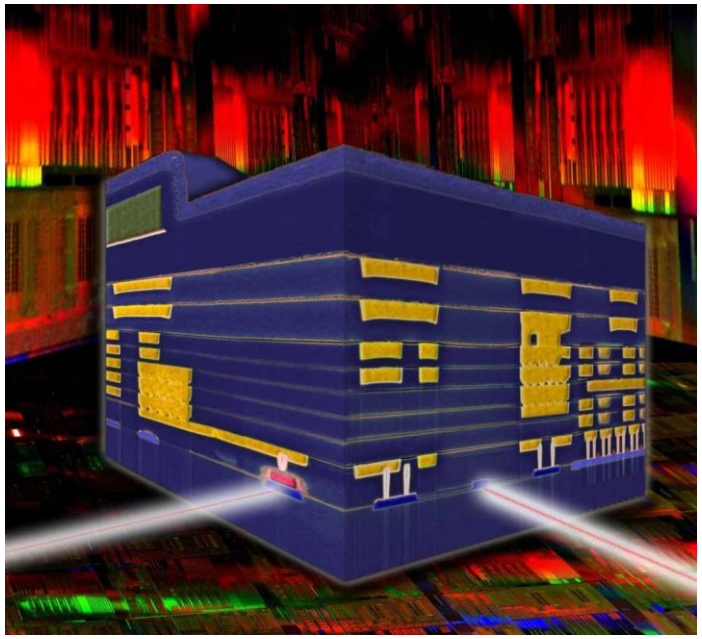
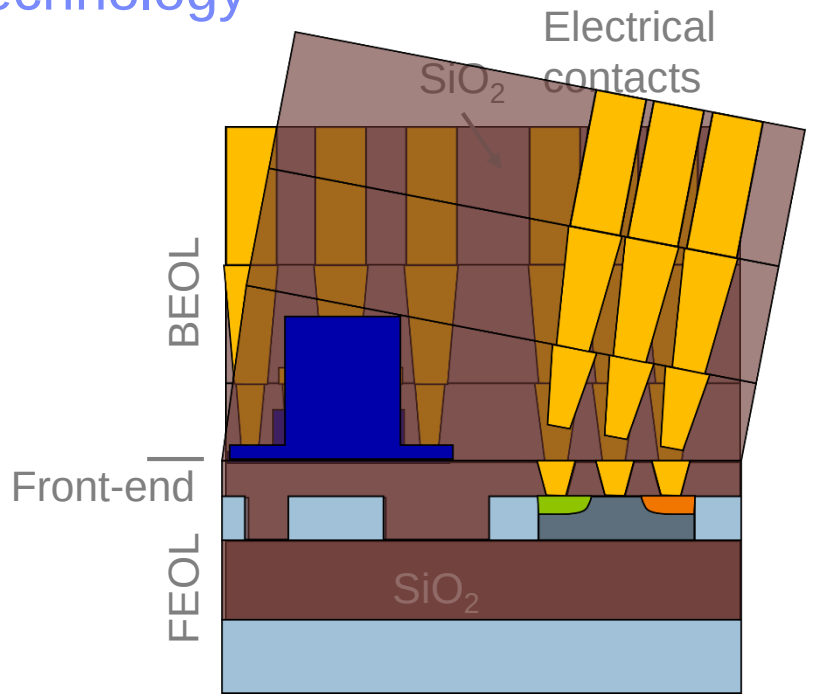
CMOS Embedded III-V on silicon technology



CMOS Si Photonics



… + III-V functionality

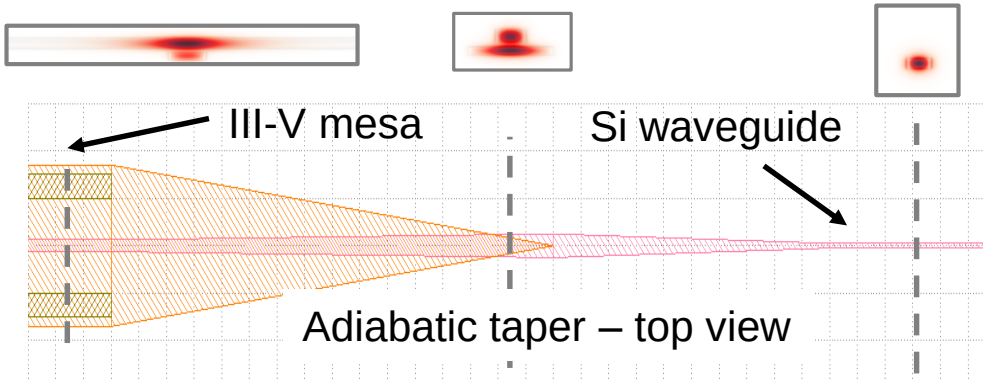
Ultra-thin III-V layer stack (300 nm) enables embedding in between FEOL and BEOL

→ **Integration of III-V functionality in the CMOS processing flow**

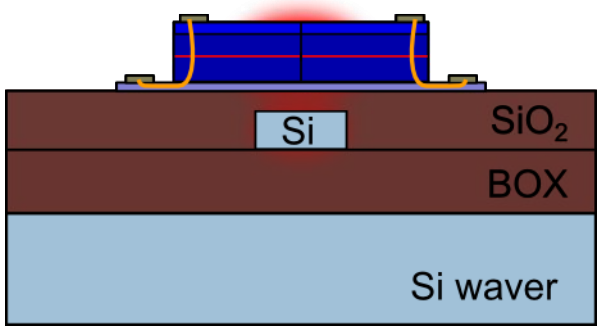
→ **Power efficient lasers for silicon photonics by high modal overlap concept**

→ **Flexible design, on-chip control and cost-effective source integration**

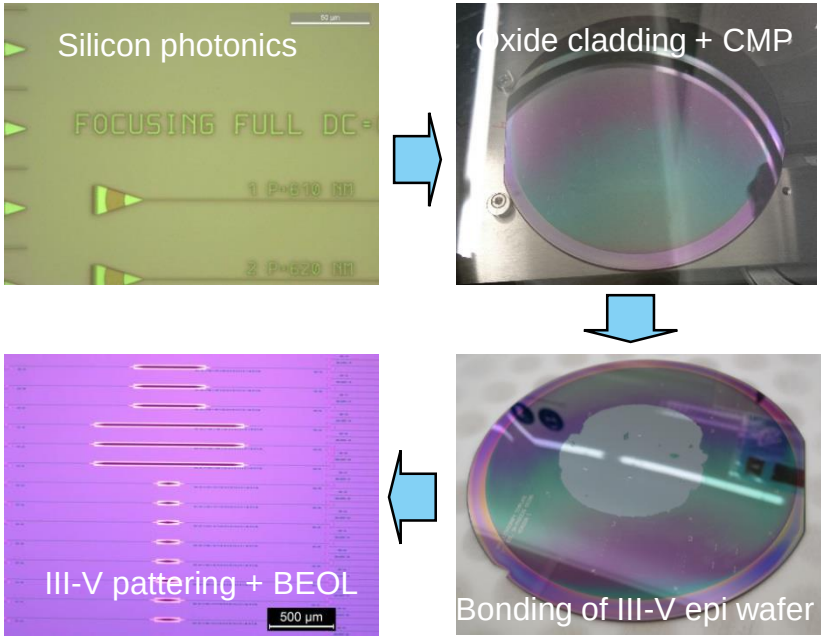
Challenges for III-V laser integration in CMOS



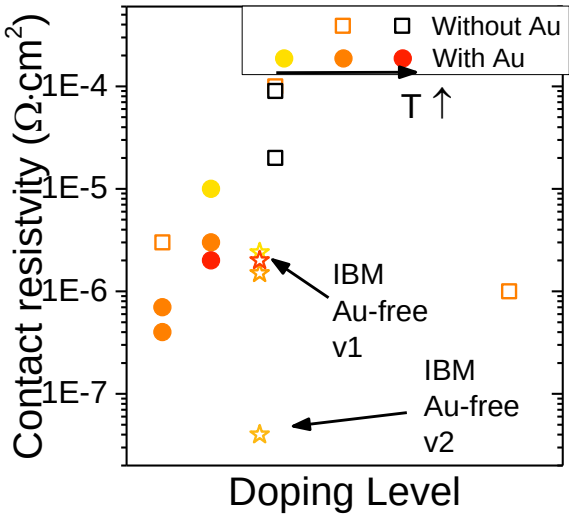
➢ III-V to silicon optical coupler



➢ Current confinement



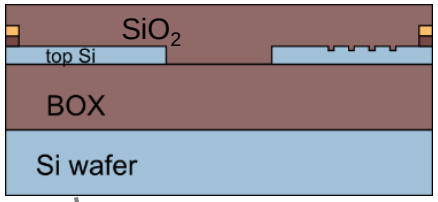
➢ Optimized process flow



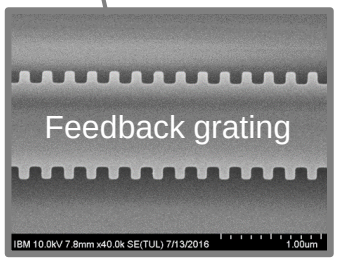
➢ CMOS-compatible Ohmic contacts on n and p-InP

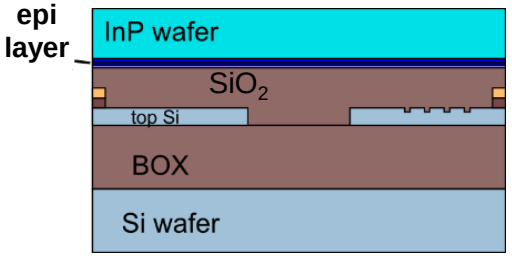
Processing scheme

- 5 InAlGaAs quantum wells (MOCVD)

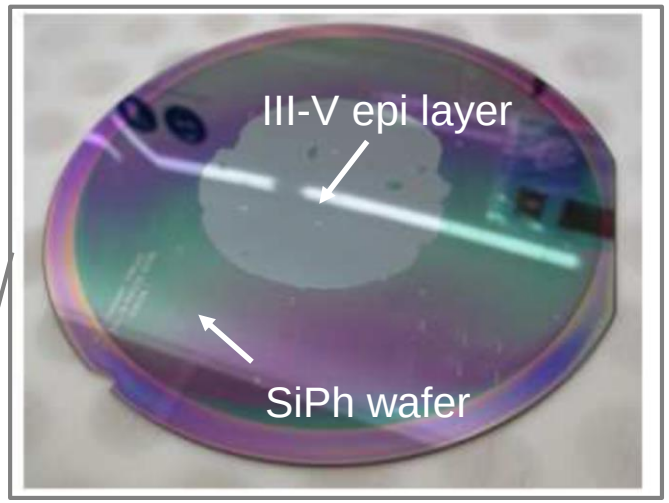


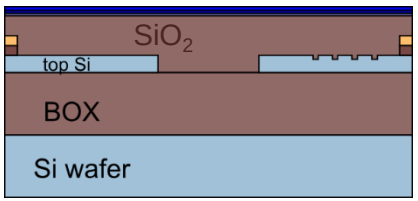
SiPh wafer



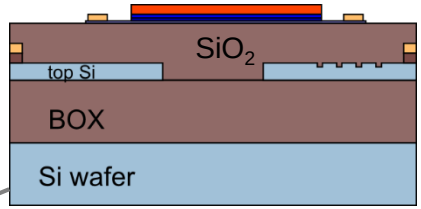


Wafer bonding

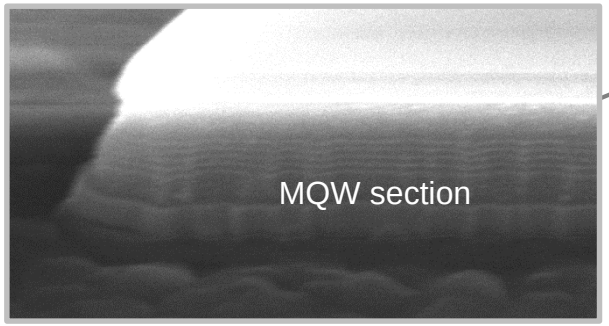


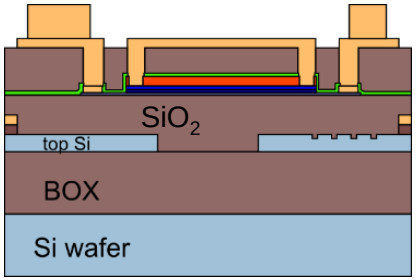


Substrate removal

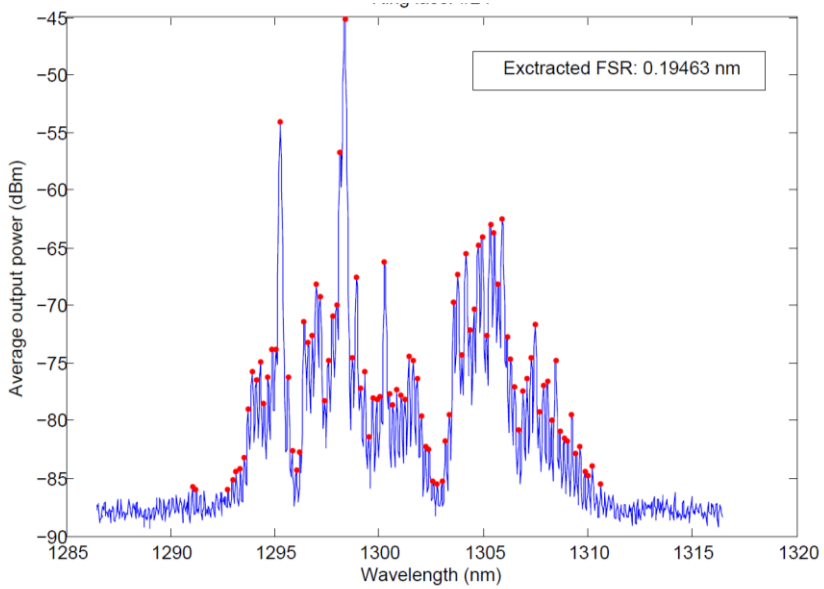


III-V structuring





Metallization

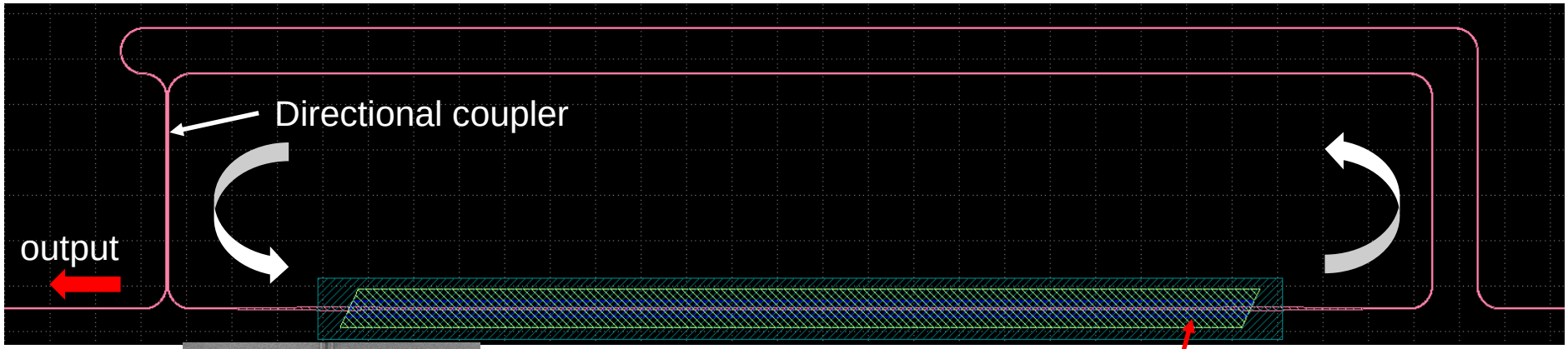


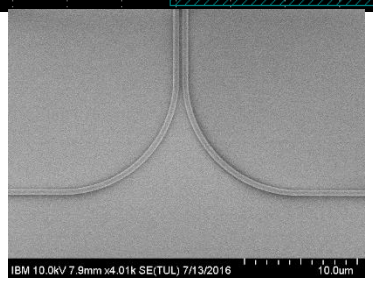
Optically pumped ring laser

Measured FSR: 0.194 nm

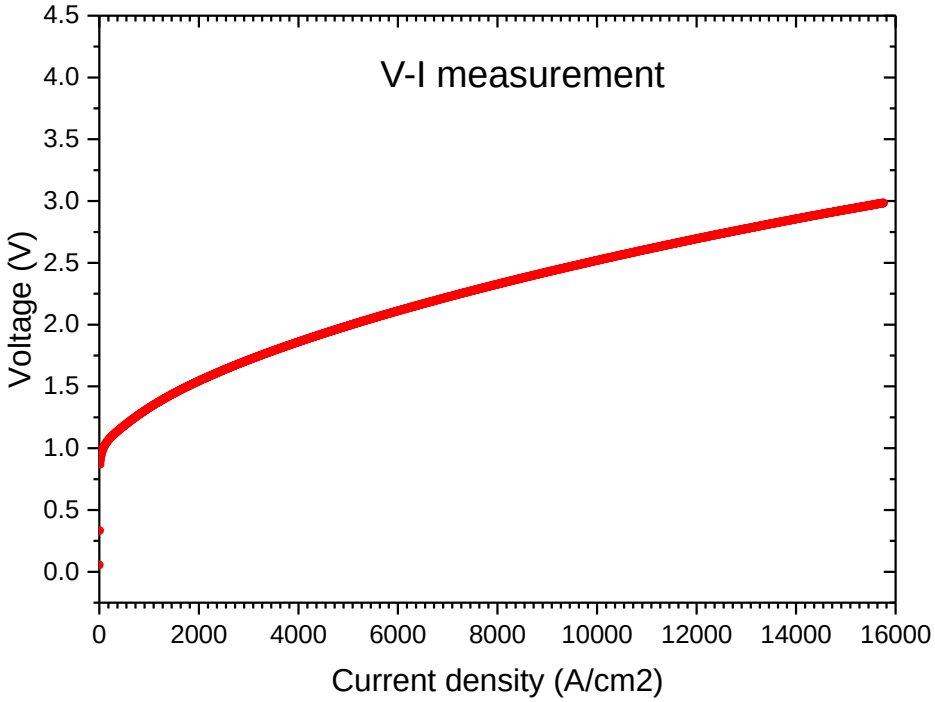
Estimated FSR from ring: 0.203 nm
Estimated FSR from III-V: 0.266 nm

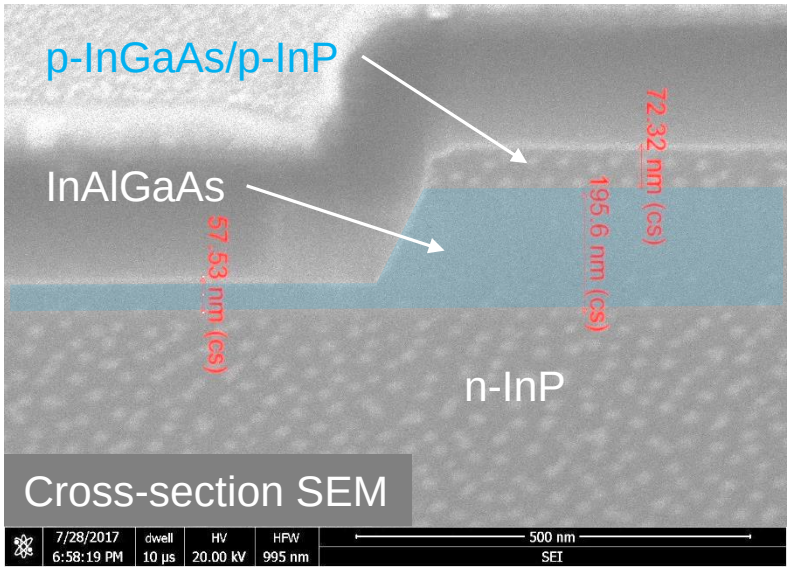
- Lasing with feedback from silicon photonics

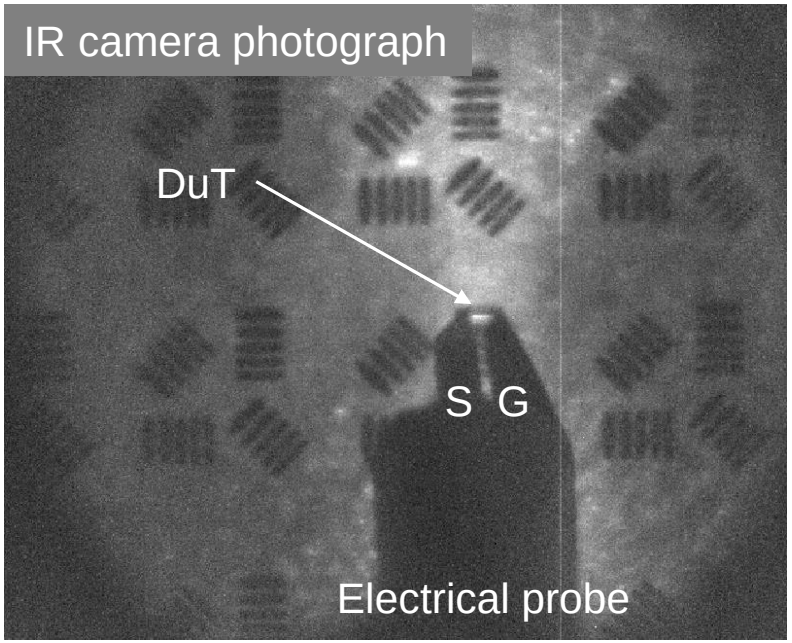




Electrically pumped LED

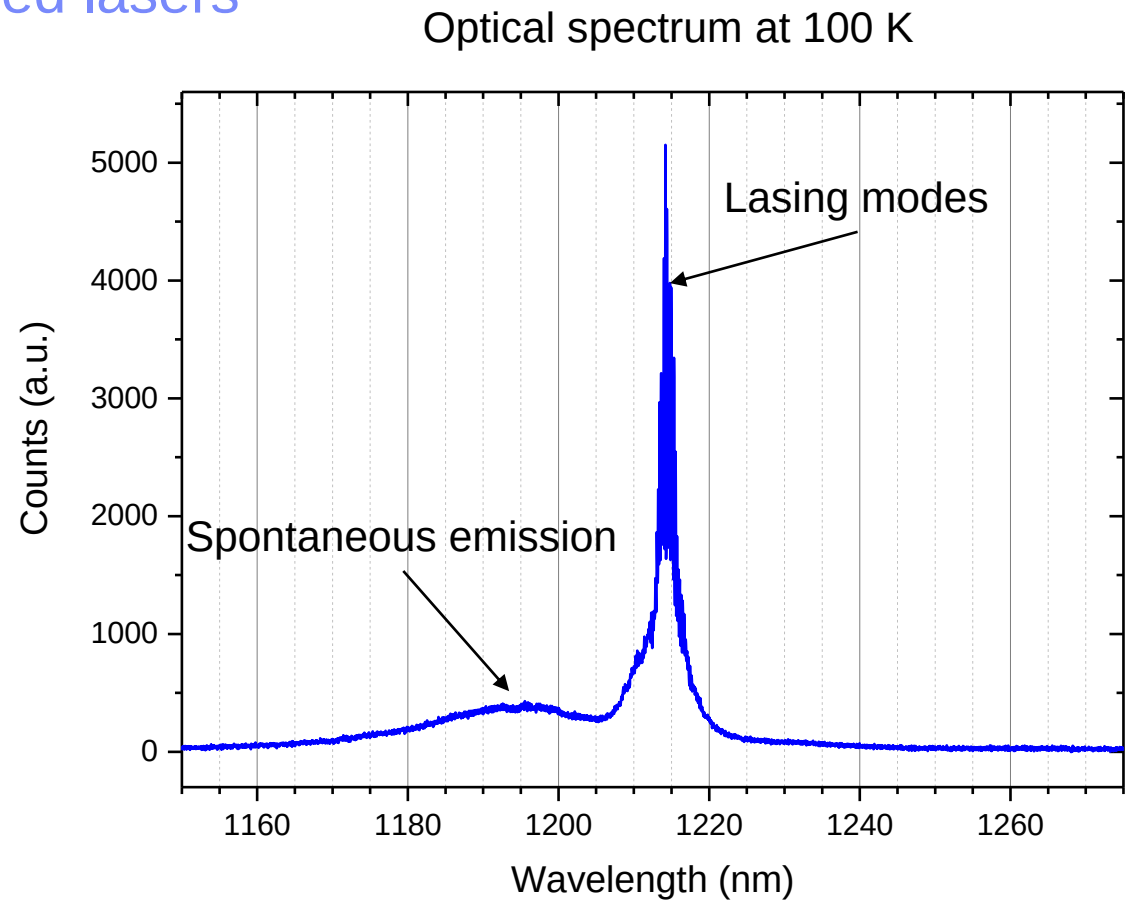






- LED test-device for process optimization
- Good V-I characteristic
- Electro-luminescence emission visible with IR-camera

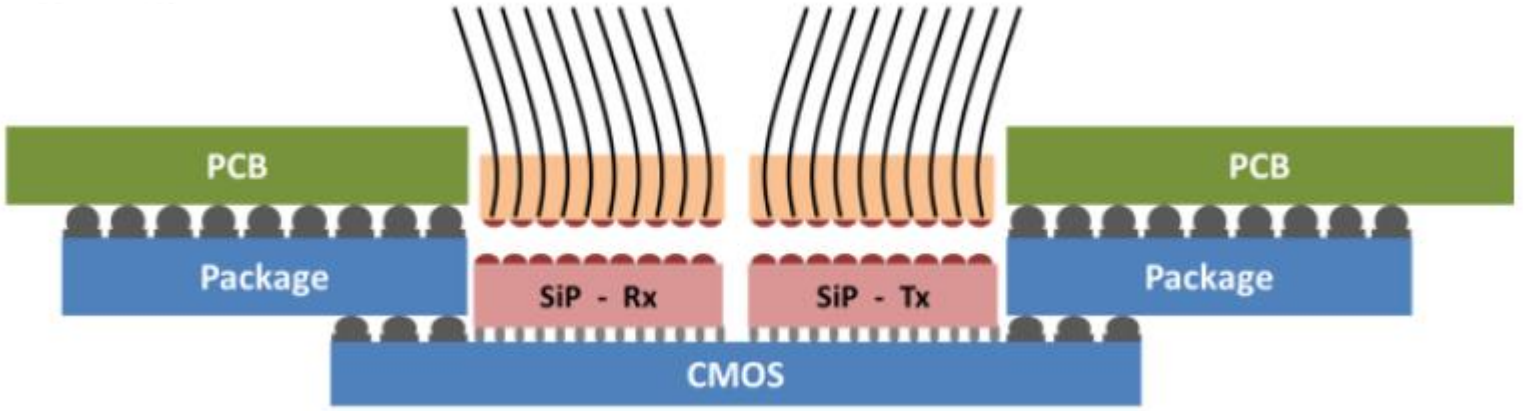
Electrically pumped lasers



- Laser devices: 10 dB optical loss at room temperature
- Cooling down increases gain
- Increased gain can overcome loss
- Pulsed electrical pumping

Work in progress !

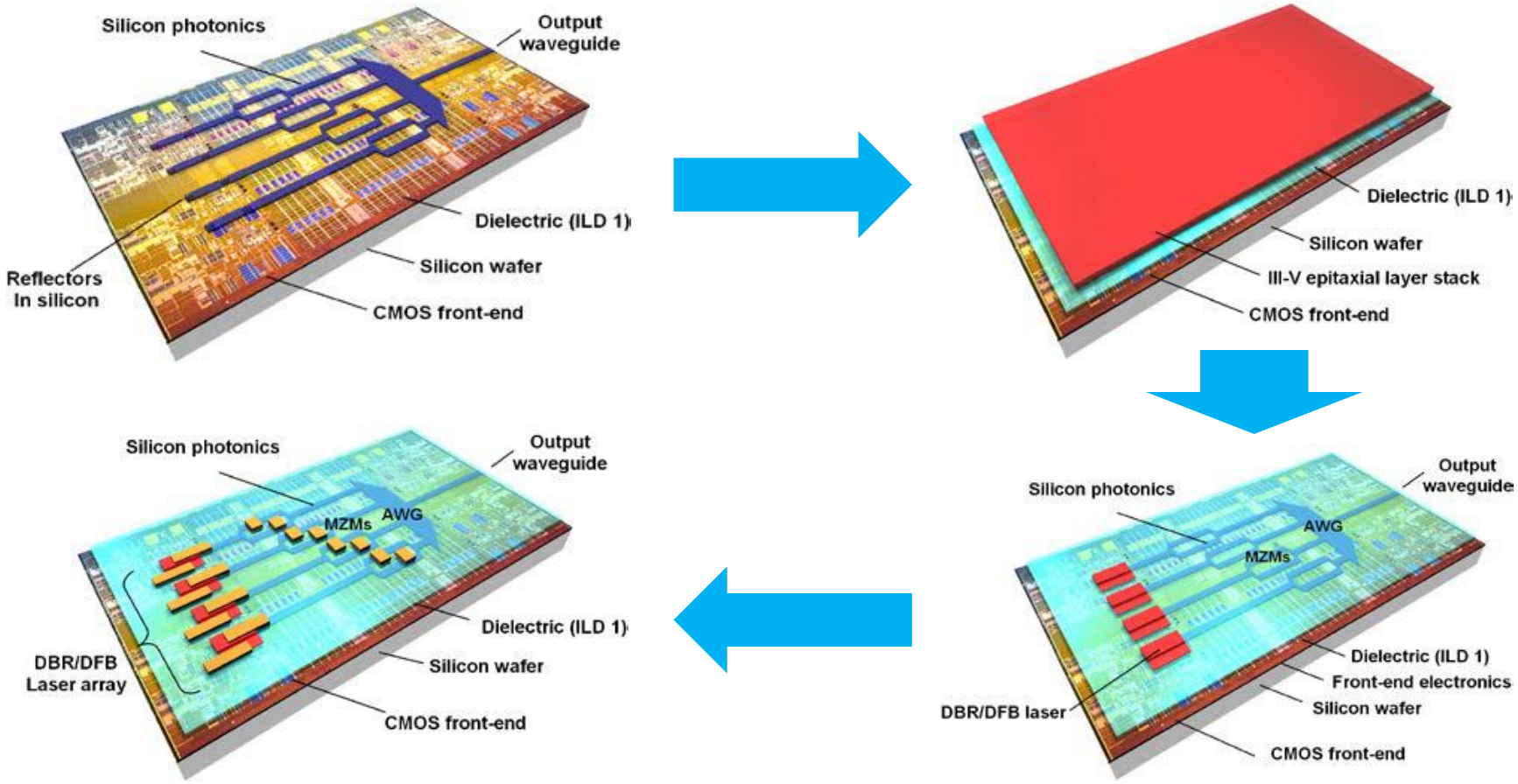
H2020 EU project L3MATRIX



- Integration: SiPh optical interconnect (8x16) with 16nm CMOS switching ASIC
- Scaling chip I/O towards Pb/s
- Silicon photonics (single-mode) → Increased reach
- Reducing network layers: less latency, more servers & memory → more throughput

- **High level of integration: Need on-chip lasers**

H2020 EU project DIMENSION



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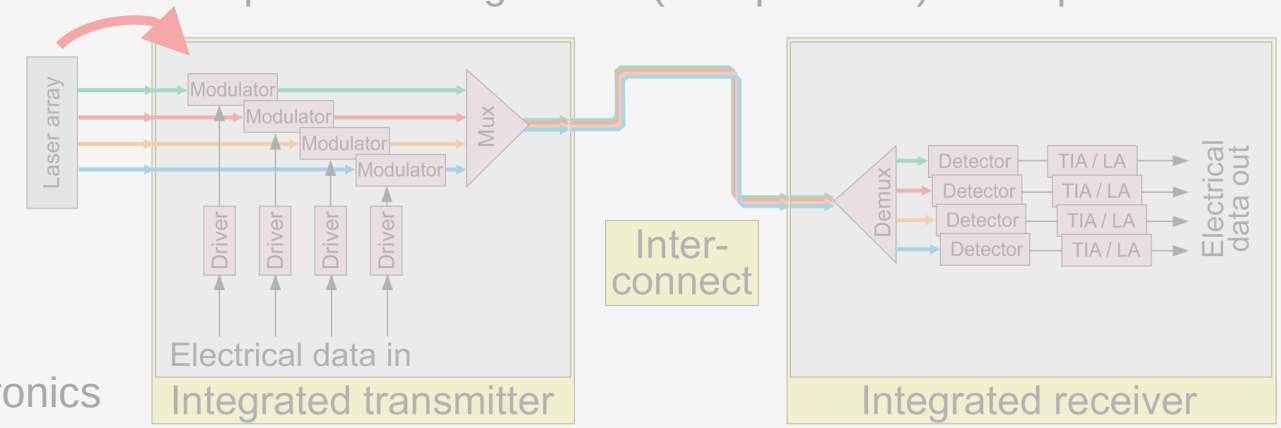

2 System-level: Scalable chip-to-fiber connectivity

- One step mating of numerous optical interfaces
- Provide electrical and optical signal routing capability
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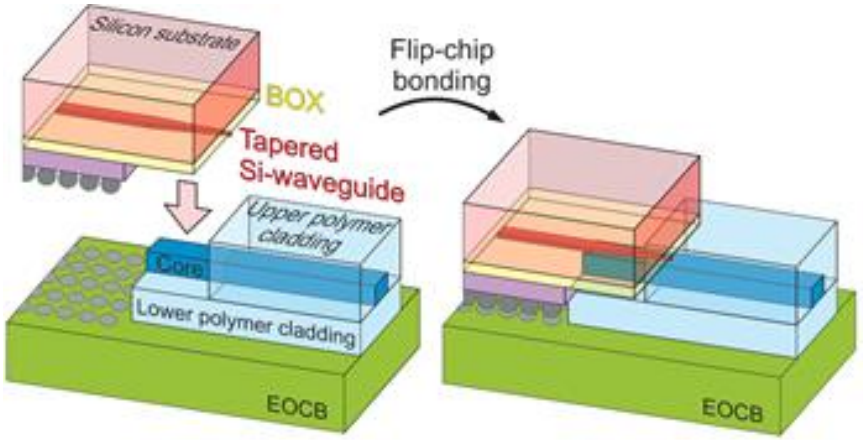
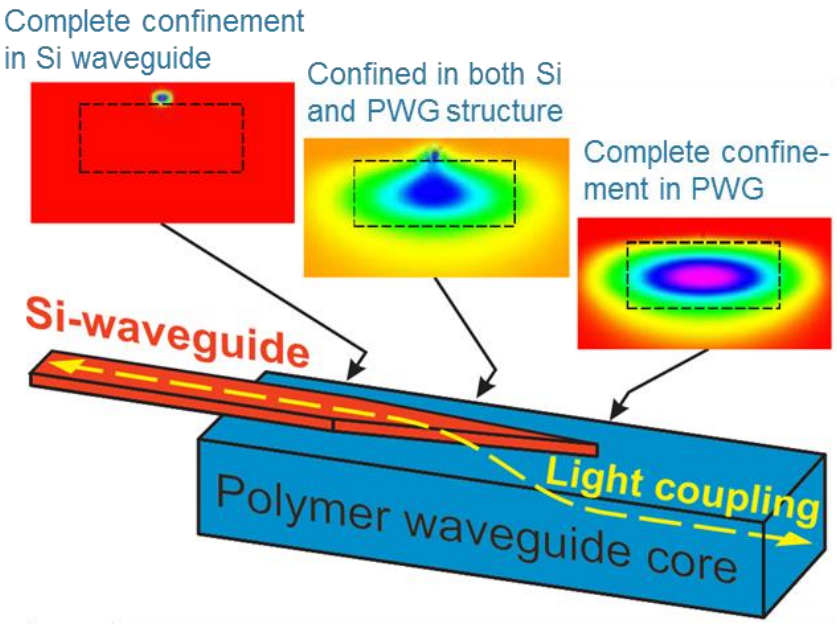
Adiabatic optical coupling using polymer waveguides

Principle:

– Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling



Schematic view of Si- photonics chip assembled by flip-chip bonding

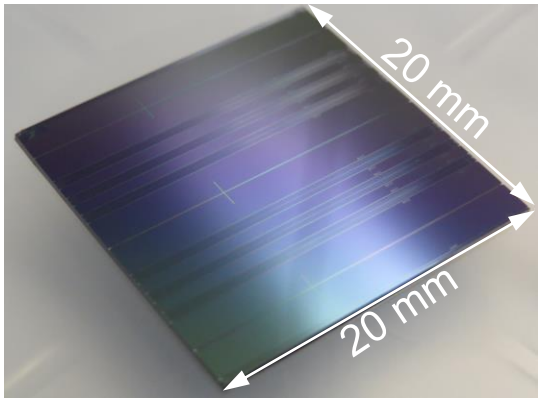


- **Compatible with established electrical assembly**
- **Simultaneous E/O interfacing**
- **Scalable to many optical channels**

- J. Shu, et al. "Efficient coupler between chip-level and board-level optical waveguides." *Optics letters* 36.18 (2011): 3614-3616.
- I. M. Soganci, et al. "Flip-chip optical couplers with scalable I/O count for silicon photonics." *Optics express* 21.13 (2013): 16075-16085.
- T. Barwicz, et al. "Low-cost interfacing of fibers to nanophotonic waveguides: design for fabrication and assembly tolerances.“, *Photonics Journal, IEEE* 6.4 (2014): 1-18.

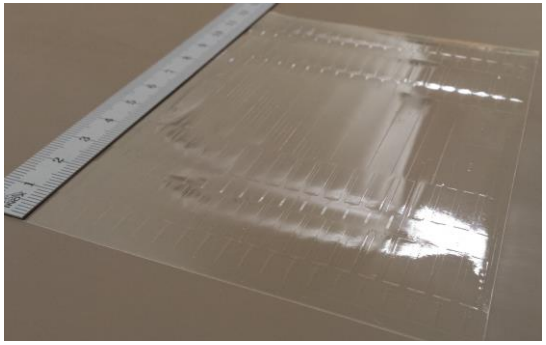
Single-mode polymer waveguide technology

SM polymer waveguides on **chips** (e.g. Si photonics chips)



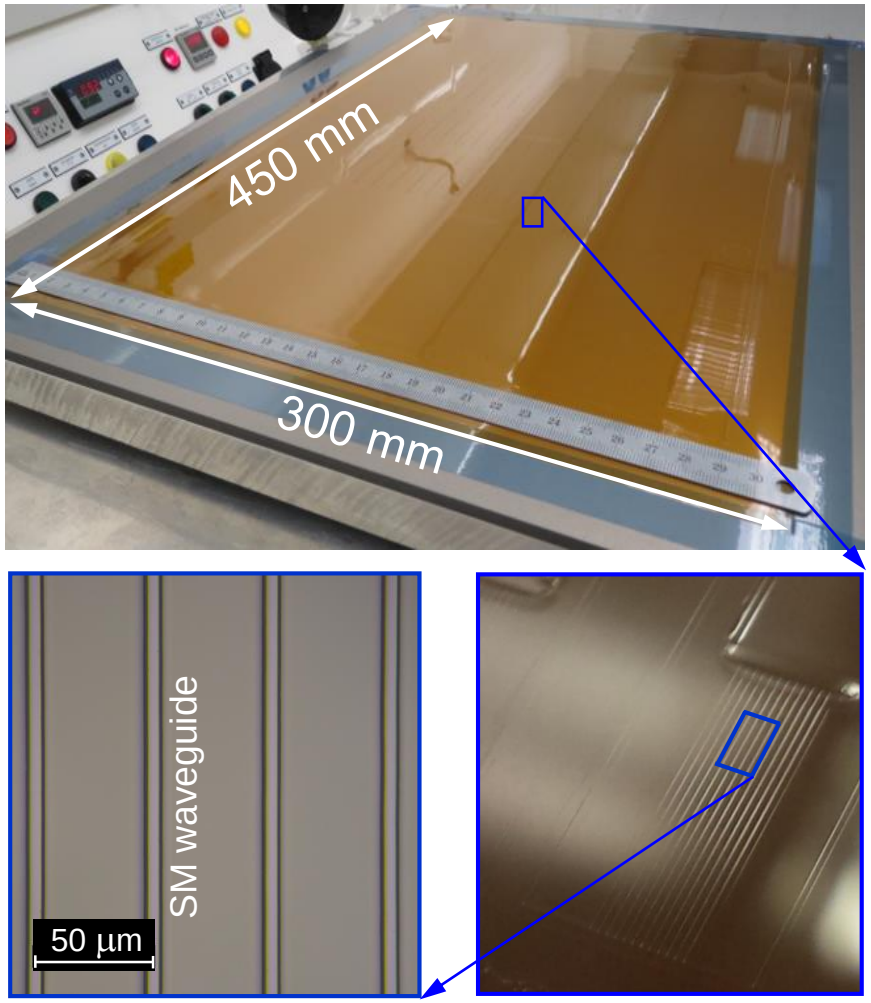
Chip-size

SM polymer waveguides on **wafer-size flexible** substrates



Wafer- size

SM polymer waveguides on **panel-size flexible** substrates



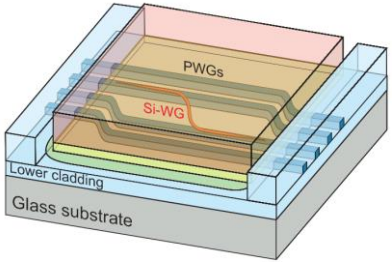
Panel-size

R. Dangel, et al. Optics Express, 2015

Insertion loss characterization (1)

Insertion loss measurement:

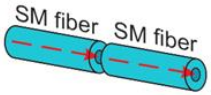
- Wavelength sweep over O-band
  - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG



Schematic view of Si-photonics chip assembled by flip-chip bonding

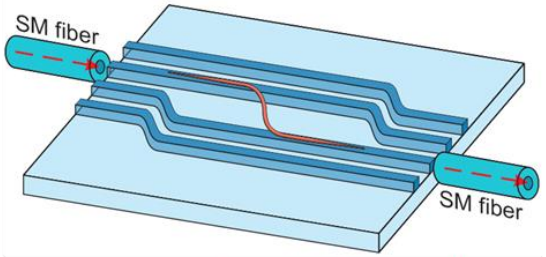
Insertion loss per 2 facets

Measurement ①

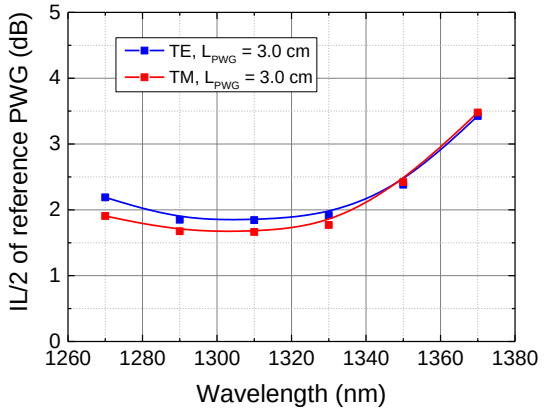


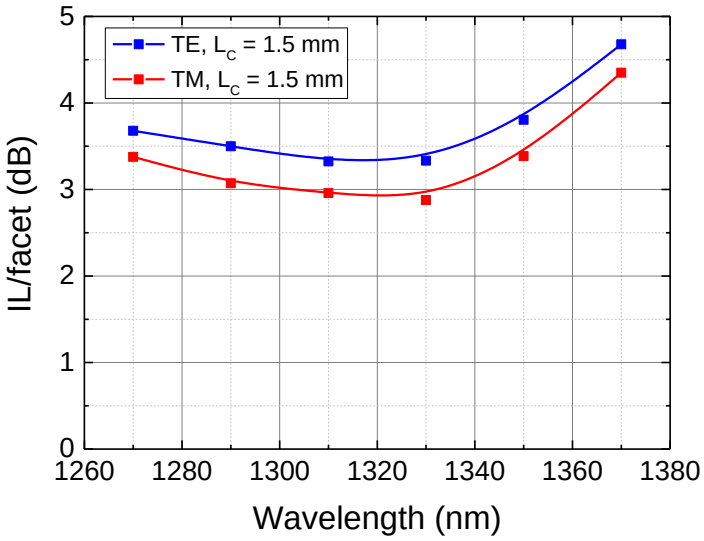
Fiber ➡ Fiber

Measurement ②



Fiber ➡ PWG ➡ SiWG ➡ PWG ➡ Fiber

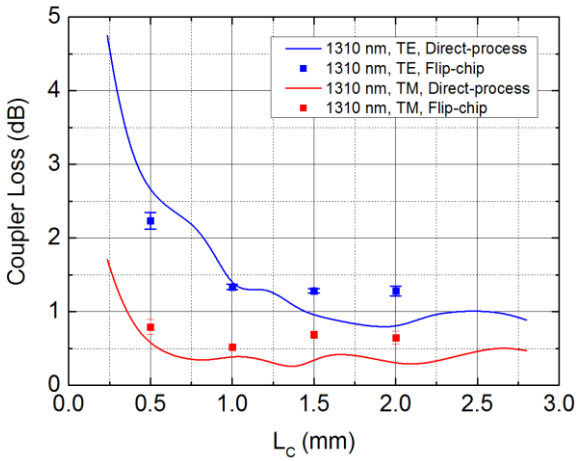


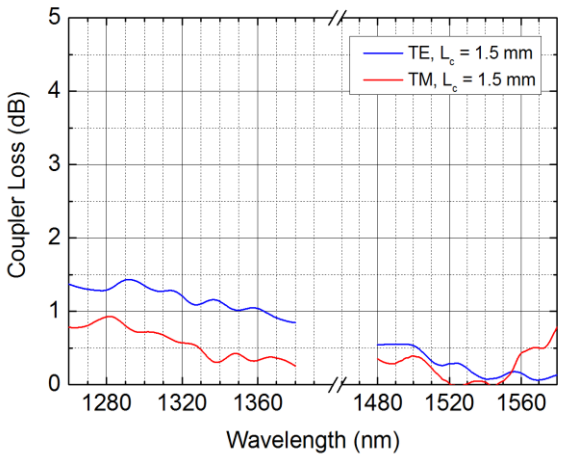


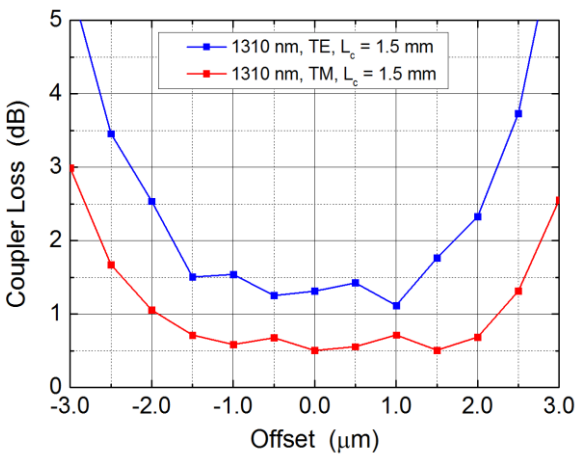
Adiabatic coupler loss characterization

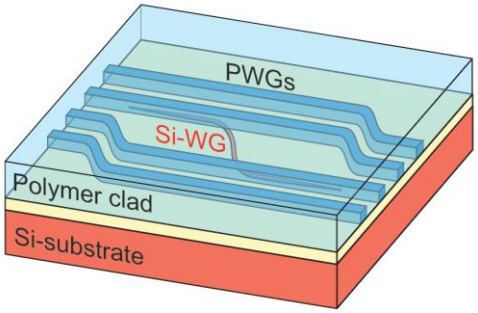
Coupler loss measurement:

- Direct-process vs Flip-chip bonding approach
- For $L_c \geq 1.0$ mm: Coupler loss < 1.5 dB, PDL ≤ 0.7 dB
- Operating in the O and C-band

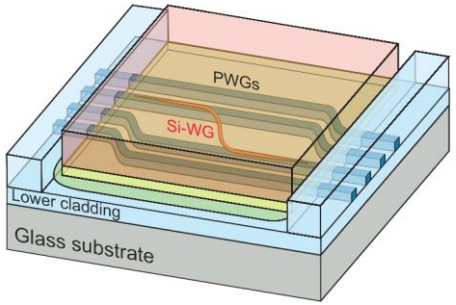






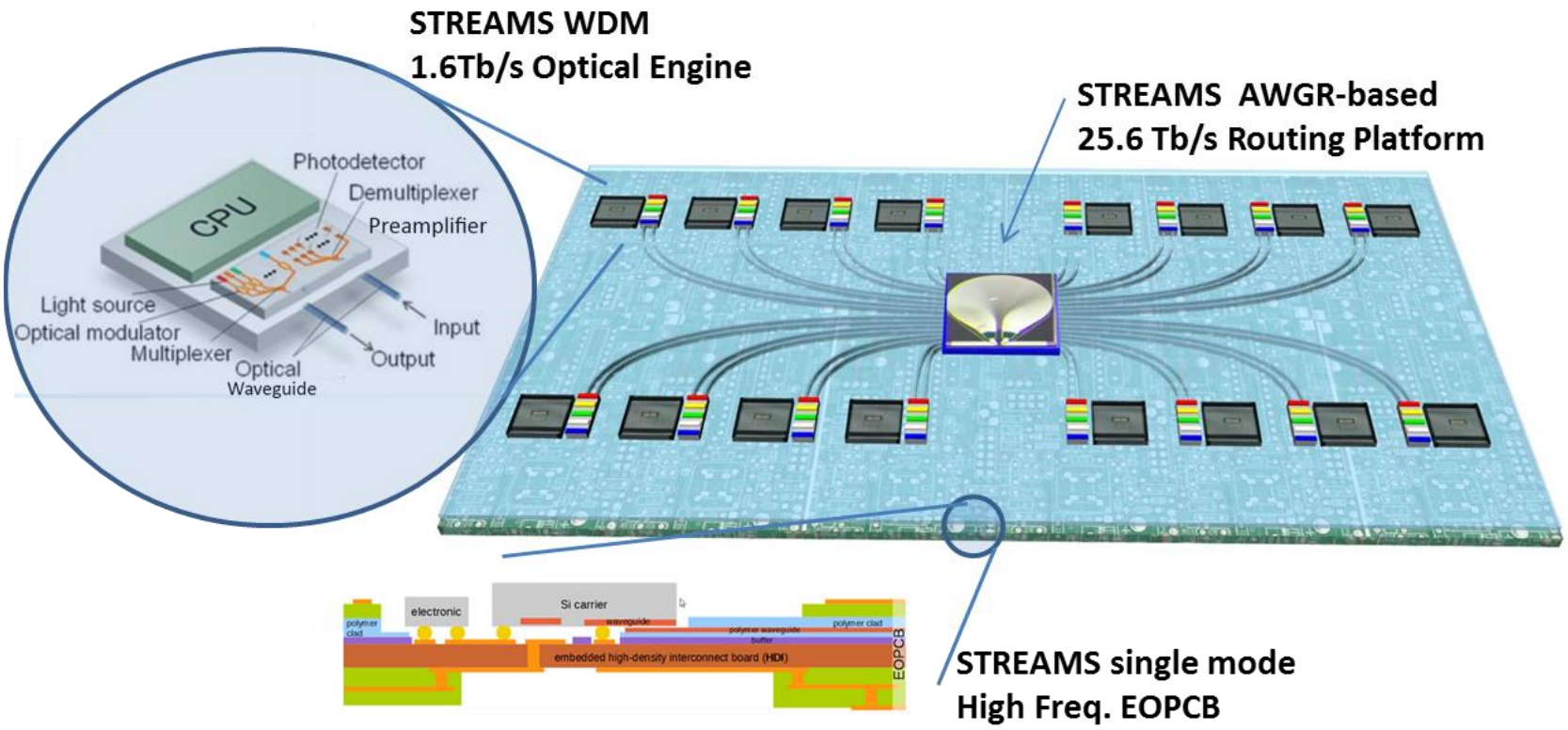


Polymer waveguides processed on chip

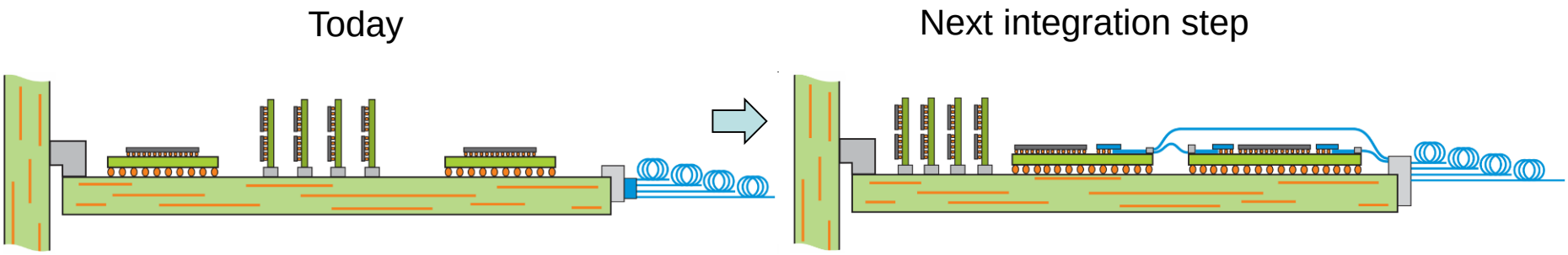


Polymer waveguides attached by flip-chip bonding

H2020 EU project ICT-STREAMS



From Si photonics transceivers to chip-level assembly



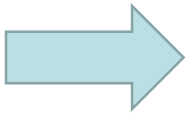
Silicon photonics co-packaging with the ASIC chip

- Less components and assembly steps
- Improved electrical signal path, reduce # interfaces and length
- High density, scalable optical IO
- Minimum overhead, lowest cost

Ultra-short electrical line. Overcome CDR and FEC
50% reduction of total link power anticipated

Summary

- **Miniaturized Photonic Packaging**
  - Chip level integration
    - CMOS+Passive+Active photonics
  - System-level integration
    - Adiabatic optical coupling as a scalable, efficient, broadband and polarization independent fiber-to-chip interfacing solution



Path towards high level of electro-optical integration & scalability

Acknowledgements

- Collaborators in IBM
  - Marc Seifried, Herwig Hahn, Gustavo Villares, Lukas Czornomaz, Folkert Horst, Daniele Caimi, Charles Caer, Yannick Baumgartner Daniel Jubin, Norbert Meier, Roger Dangel, Antonio La Porta, Jonas Weiss, Jean Fompeyrine, Ute Drechsler
  - And many others

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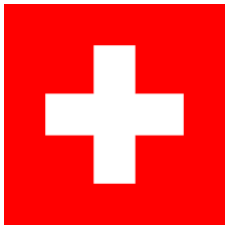
- The opinion expressed and arguments employed herein do not necessarily reflect the official views of the Swiss Government.



Agreement No 688003 Contract No 15.0313

Agreement No 688172 Contract No 15.0339

Agreement No 688544 Contract No 15.0346

Agreement No 688572 Contract No 15.0309

Thank you for your attention

- Bert Jan Offrein
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