Chip and system-level integration technologies for silicon photonics

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5th International Symposium for Optical Interconnect in Data Centres
Outline

• The need for integration at component and system level
  – CMOS silicon photonics with embedded III-V materials
  – High channel count silicon photonics packaging
• Summary
Communication between two processors

Optical communication:
- 1000 x Larger bandwidth
- 1000 x Lower loss
- 100 x Larger distance

Optical communication requires many more components and assembly steps !!!
Photonics technologies for system-level integration

1. **Chip-level**: CMOS silicon photonics + Active photonics devices
   - Si photonics provides all required building blocks (except lasers) on chip-level:
     - Modulators
     - Drivers
     - Detectors
     - Amplifiers
     - WDM filters
   + CMOS electronics

2. **System-level**: Scalable chip-to-fiber connectivity
   - One step mating of numerous optical interfaces
   - Provide electrical and optical signal routing capability
   - Enable a simultaneous interfacing of electrical and optical connections
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CMOS Embedded III-V on silicon technology

Ultra-thin III-V layer stack (300 nm) enables embedding in between FEOL and BEOL

→ Integration of III-V functionality in the CMOS processing flow
→ Power efficient lasers for silicon photonics by high modal overlap concept
→ Flexible design, on-chip control and cost-effective source integration
Challenges for III-V laser integration in CMOS

- Current confinement
- III-V to silicon optical coupler
- Optimized process flow

Contact resistivity (Ω·cm²) vs. Doping Level

- Without Au
- With Au
- IBM Au-free v1
- IBM Au-free v2
Processing scheme

- 5 InAlGaAs quantum wells (MOCVD)
- III-V epi layer
- SiPh wafer
- Wafer bonding
- Substrate removal
- III-V structuring
- Metallization
Optically pumped ring laser

Measured FSR: 0.194 nm

Estimated FSR from ring: 0.203 nm
Estimated FSR from III-V: 0.266 nm

- Lasing with feedback from silicon photonics
Electrically pumped LED

- LED test-device for process optimization
- Good V-I characteristic
- Electro-luminescence emission visible with IR-camera
Electrically pumped lasers

- Laser devices: 10 dB optical loss at room temperature
- Cooling down increases gain
- Increased gain can overcome loss
- Pulsed electrical pumping

Optical spectrum at 100 K

Work in progress!
H2020 EU project L3MATRIX

- Integration: SiPh optical interconnect (8x16) with 16nm CMOS switching ASIC
- Scaling chip I/O towards $Pb/s$
- Silicon photonics (single-mode) $\rightarrow$ Increased reach
- Reducing network layers: less latency, more servers & memory $\rightarrow$ more throughput

- High level of integration: Need on-chip lasers
H2020 EU project DIMENSION
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Adiabatic optical coupling using polymer waveguides

Principle:
- Contact between the silicon waveguide taper and the polymer waveguide (PWG), achieved by flip-chip bonding, enables adiabatic optical coupling

- Compatible with established electrical assembly
- Simultaneous E/O interfacing
- Scalable to many optical channels

Single-mode polymer waveguide technology

SM polymer waveguides on **chips** (e.g. Si photonics chips)

SM polymer waveguides on **panel-size flexible** substrates

SM polymer waveguides on **wafer-size flexible** substrates

Insertion loss characterization (1)

Insertion loss measurement:
- Wavelength sweep over O-band
  - Full path vs ref. PWG path
- Wavelength dependency mainly in the PWG

Insertion loss per 2 facets

Measurement ①

Measurement ②
Adiabatic coupler loss characterization

**Coupler loss** measurement:

- Direct-process vs Flip-chip bonding approach
- For $L_c \geq 1.0$ mm: Coupler loss $< 1.5$ dB, PDL $\leq 0.7$ dB
- Operating in the O and C-band
H2020 EU project ICT-STREAMS

STREAMS WDM
1.6Tb/s Optical Engine

STREAMS AWGR-based
25.6 Tb/s Routing Platform

STREAMS single mode
High Freq. EOPCB
From Si photonics transceivers to chip-level assembly

Silicon photonics co-packaging with the ASIC chip
- Less components and assembly steps
- Improved electrical signal path, reduce # interfaces and length
- High density, scalable optical IO
- Minimum overhead, lowest cost

Ultra-short electrical line. Overcome CDR and FEC
50% reduction of total link power anticipated
Summary

• **Miniaturized Photonic Packaging**
  – Chip level integration
    • CMOS+Passive+Active photonics
  – System-level integration
    • Adiabatic optical coupling as a scalable, efficient, broadband and polarization independent fiber-to-chip interfacing solution

Path towards high level of electro-optical integration & scalability
Acknowledgements

• Collaborators in IBM
  – Marc Seifried, Herwig Hahn, Gustavo Villares, Lukas Czornomaz, Folkert Horst, Daniele Caimi, Charles Caer, Yannick Baumgartner Daniel Jubin, Norbert Meier, Roger Dangel, Antonio La Porta, Jonas Weiss, Jean Fompeyrine, Ute Drechsler
  – And many others

• Co-funded by the European Union Horizon 2020 Programme and the Swiss National Secretariat for Education, Research and Innovation (SERI)

• The opinion expressed and arguments employed herein do not necessarily reflect the official views of the Swiss Government.
Thank you for your attention

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