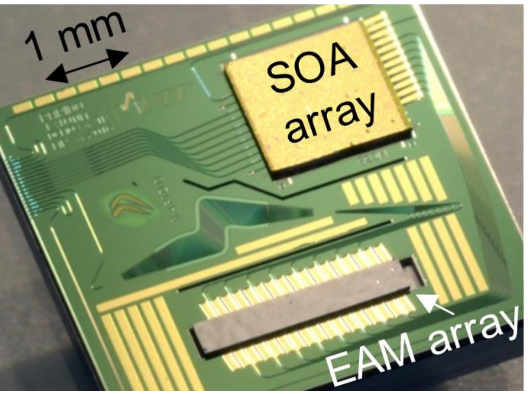


Silicon photonics on 3 and 12 µm thick SOI for optical interconnects

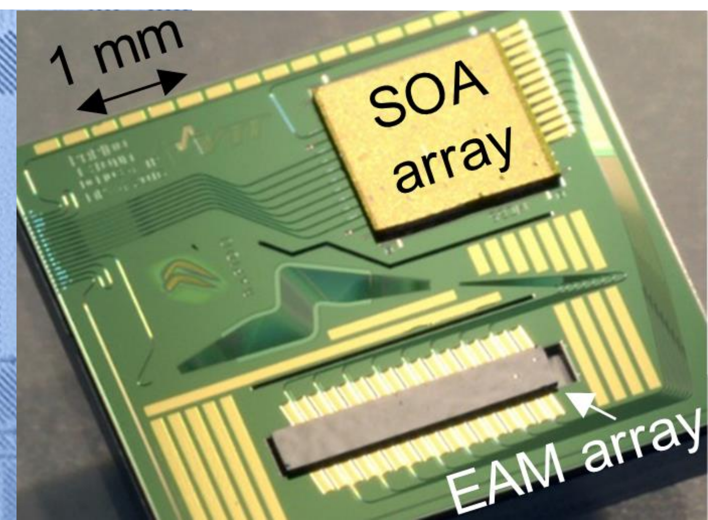
Timo Aalto

VTT Technical Research Centre of Finland

5th International Symposium for Optical Interconnect in Data Centres in ECOC, Gothenburg, 19 September 2017

Outline

- Introduction to VTT and the Thick-SOI technology
- Hybrid integration of III-V optoelectronics with Si photonics (for optical interconnects etc.)
- Latest advances in monolithic integration on 3 µm SOI
- Faraday rotation in 3 µm SOI waveguides
- Conclusions & Outlook

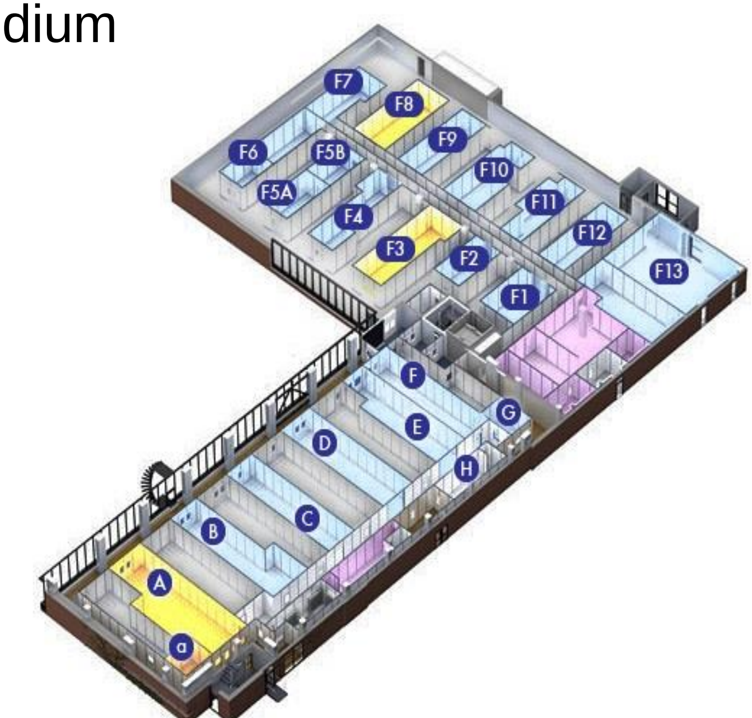


VTT Technical Research Center of Finland Ltd.

- Leading research and technology company in the Nordic countries
- A state-owned, non-profit limited liability company
- Expert services for domestic & international customers

, including MPW and dedicated runs for Si photonics

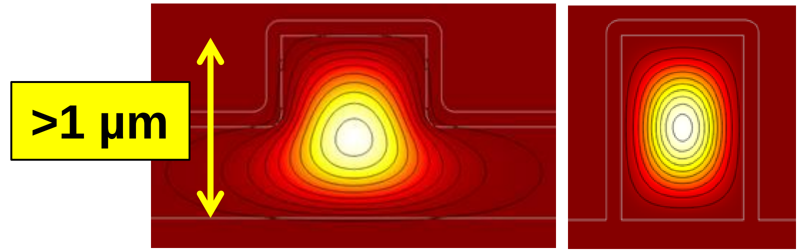
- Contract manufacturing services for small and medium volume by VTT Memsfab Ltd. (incl. Si photonics)
- Micronova clean room: 150 mm wafers, 2 600 m^2

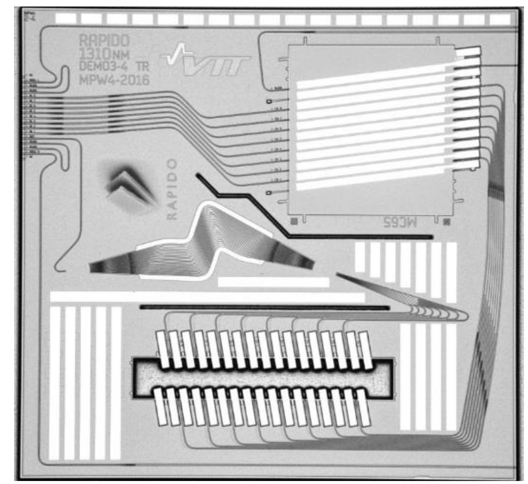


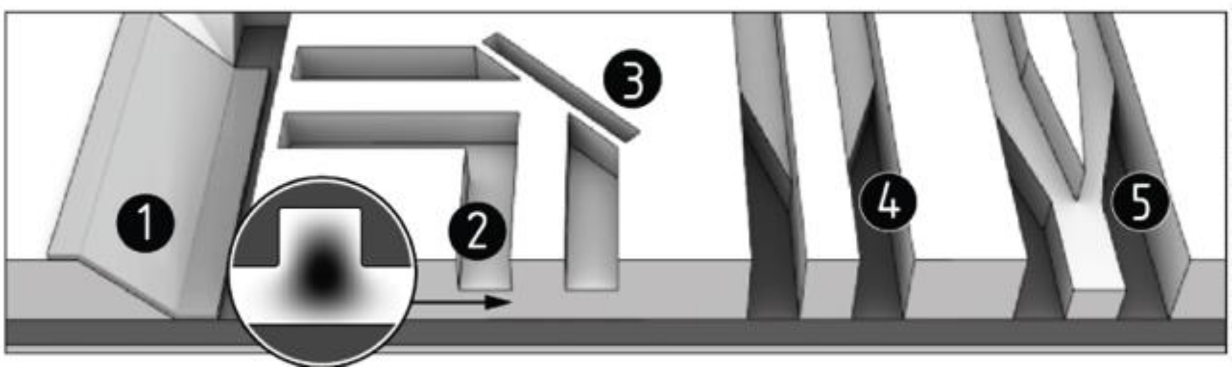
http://www.freeworldmaps.net/europe/finland/location.html

Combination of two complementary waveguide structures on 3–12 µm SOI

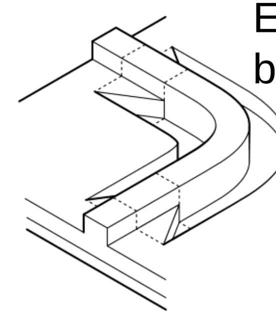
- Rib waveguides for single-mode operation
- Strip waveguides for dense integration
- Adiabatic rib-strip coupling
- Polarization independent operation
- Tolerates watt-level optical powers
- Low-loss waveguides and passive components
- Hybrid integration of active components
- Monolithic photodiodes and modulators under development







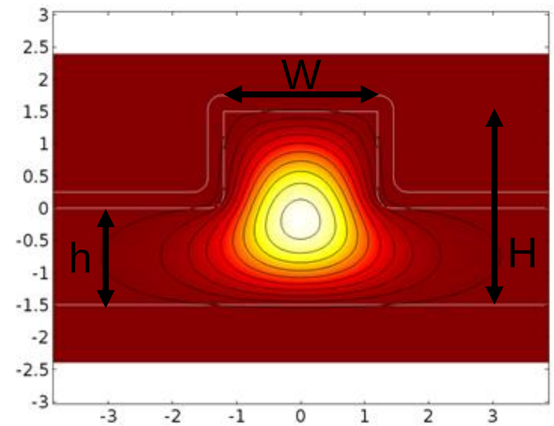
1. Metal mirror
2. Rib waveguide
3. TIR mirror
4. Rib-strip converter
5. Vertical taper



Euler bend

Basics of rib waveguides

- Wavelength independent single-mode operation (covering the whole 1.2 - 6 μm wavelength range)
  - Width limit: $$\frac{W}{H} < 0.3 + \frac{h/H}{\sqrt{1-(h/H)^2}}$$
  - Height ratio limit: h ≥ H/2
  - Absolute size: H ≥ 2λ

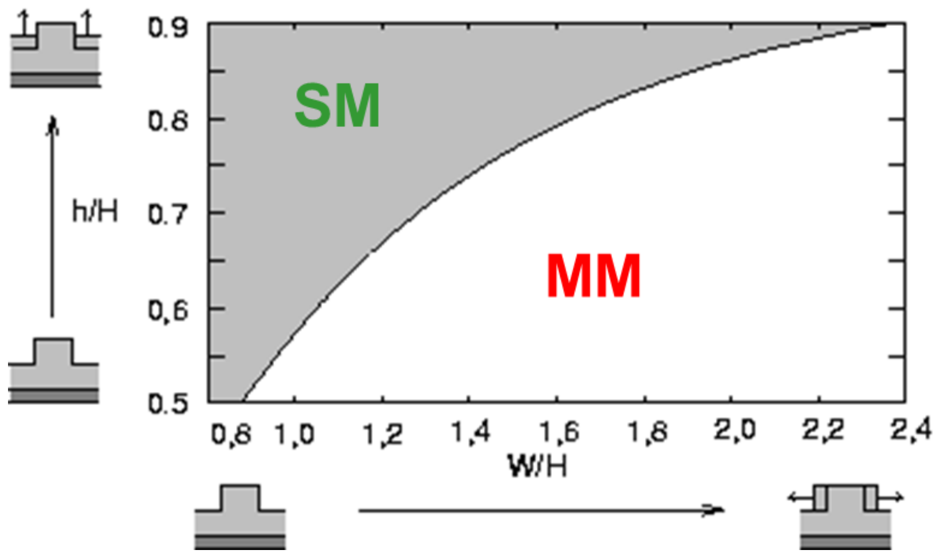


Benefits:

- Small propagation loss (0.1 dB/cm)
- Small birefringency ($\Delta n_{eff} \sim 10^{-3}$)
- SM operation over ultra-wide bandwidth

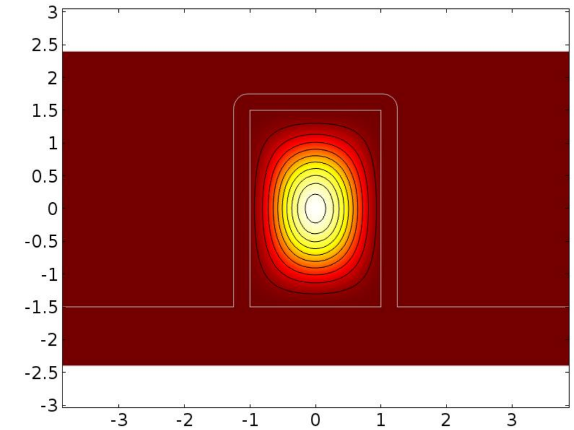
Limitations:

- Large bending radius (mm/cm scale)
- Cross-talk between waveguides



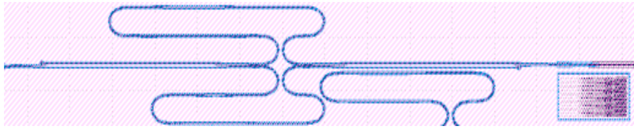
Basics of strip waveguides

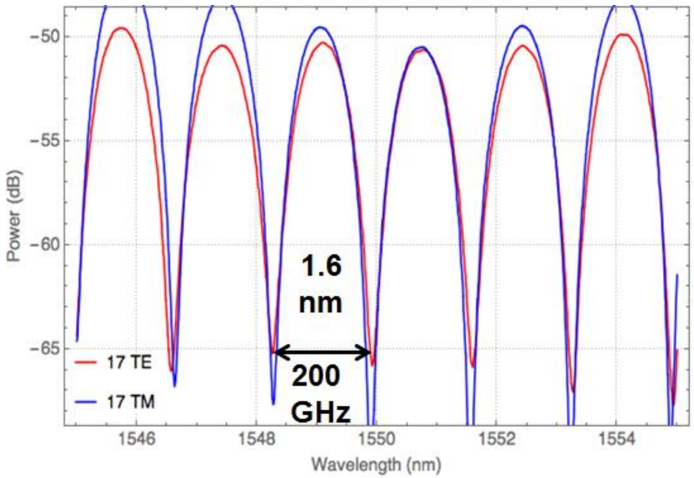
- Highly multi-moded (MM) waveguides
- Can be used in SM waveguide circuits **IF** light is kept in the fundamental mode
  - Adiabatic rib-strip converters are a key component



Benefits:

- Small propagation loss (0.1-0.15 dB/cm)
- Zero birefringence possible
- Euler bends reaching down to 1 µm bending radius
- No cross-talk between waveguides (dense arrays)





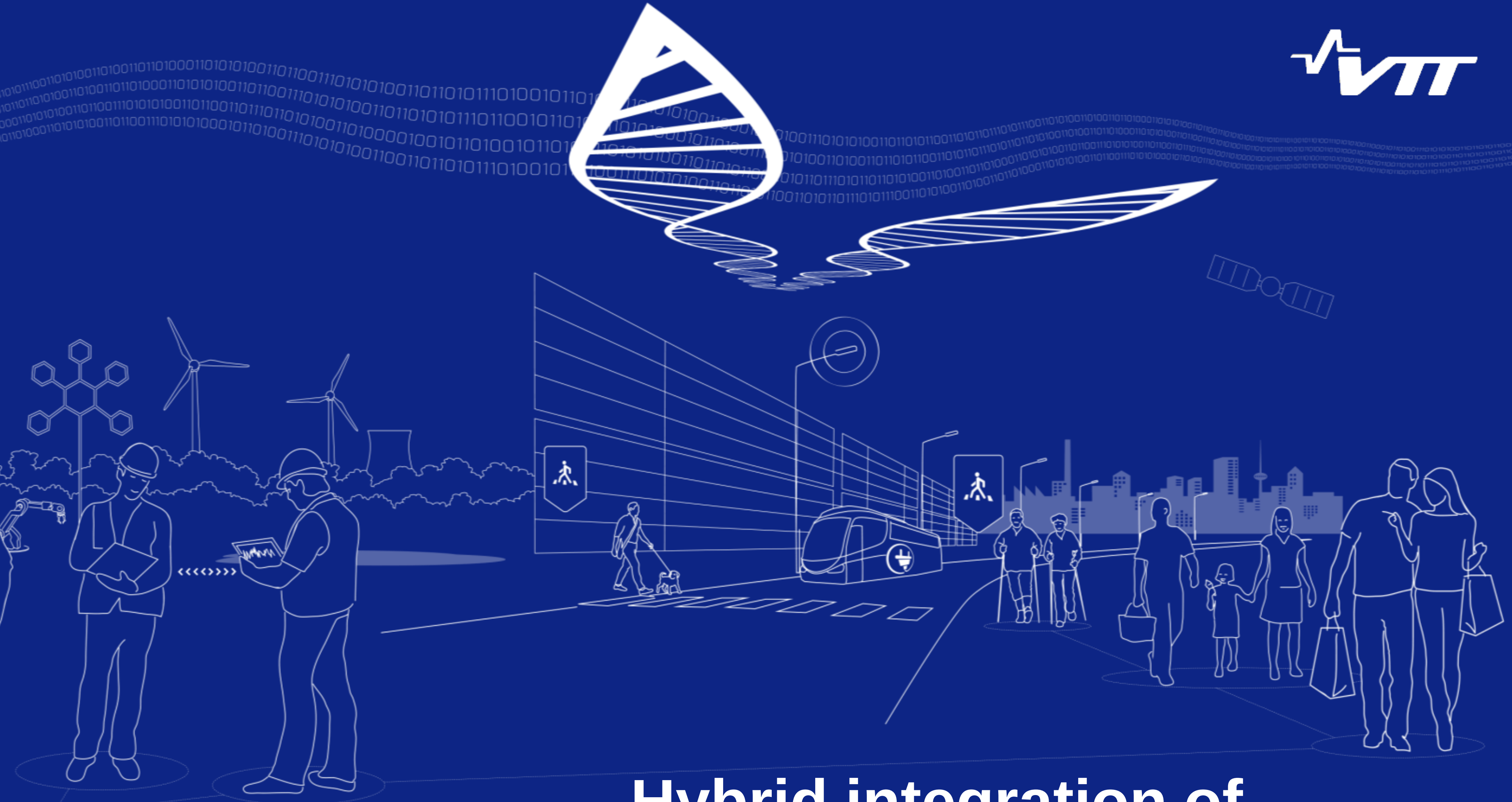
Limitations:

- Excitation of higher-order modes needs to be avoided

MEASURED PERFORMANCE EXAMPLES ON SOI

Values given for the worse polarisation

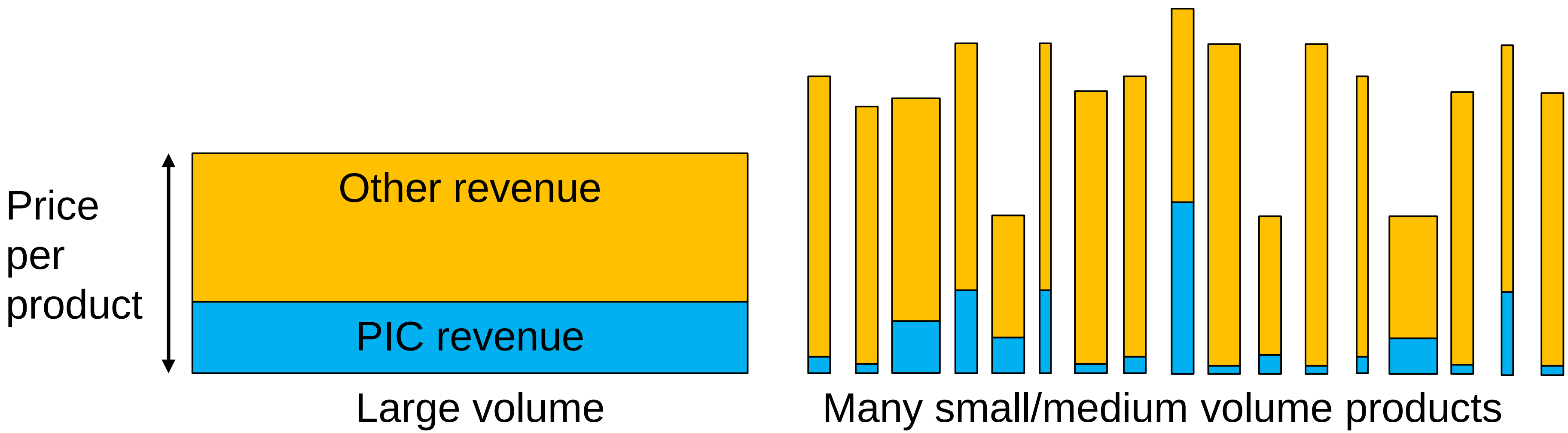
Component	Performance	Property
SOI rib and strip waveguides	0.1 dB/cm	Propagation loss
Rib-strip converter	0.05 dB	Insertion loss
Horizontal mirror	0.08 dB/90°	Insertion loss
Waveguide bends		
Ultra small (R_{eff} 1.3 µm)	0.2 dB/90°	Insertion loss
Low-loss (R_{eff} 6 µm)	<0.03 dB/90°	Insertion loss
2×2 coupler	0.3 dB	Insertion loss
TO switching/tuning	<1 µs	Response time
Polarisation splitter	>10 dB	Extinction ratio
Wavelength (de)multiplexers	2-6 dB 20-30 dB	Insertion loss Extinction ratio



Hybrid integration of III-V optoelectronics with Si photonics

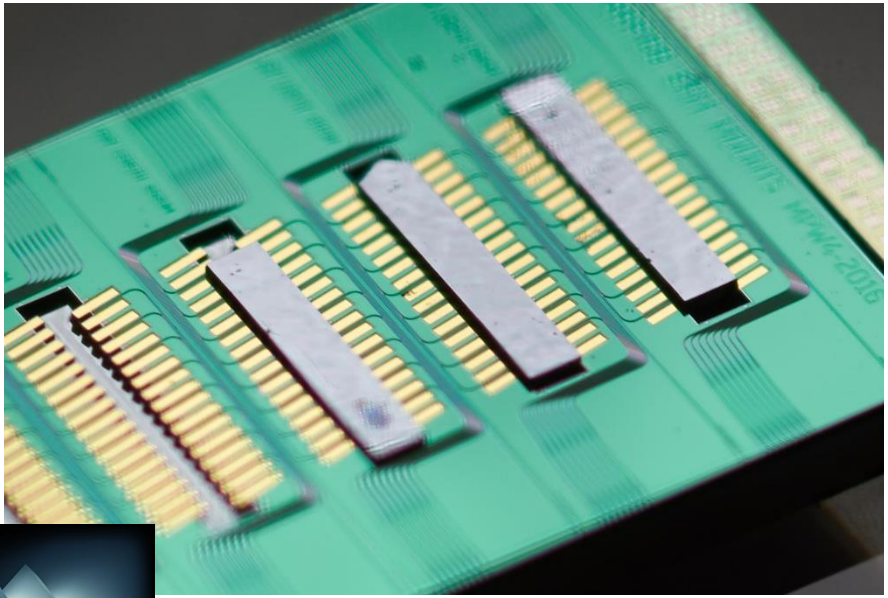
Why to use III-V hybrid integration on SOI instead of monolithic integration?

- Both hybrid and monolithic approaches are needed to fulfil all the different needs for photonics integration!
- Monolithic approach is preferred in highest-volume applications
- Hybrid approaches provide agile solutions to large number of small & medium volume applications where
  - PIC cost is typically small compared to overall product price
  - Total PIC-enabled revenue can become large

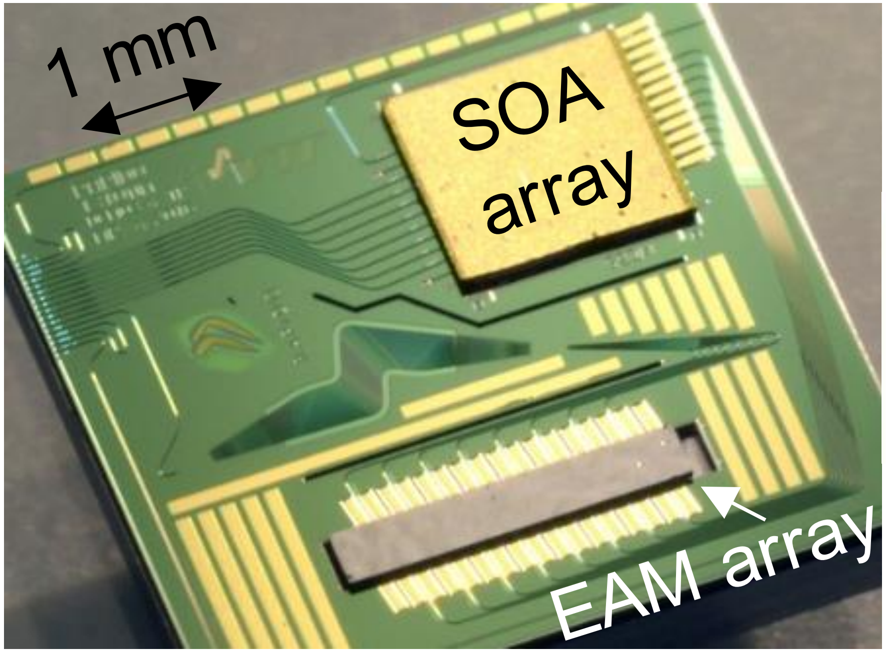


Flip-chip bonding of III-V dies on SOI

- Submicron flip-chip accuracy with Au-Au thermo compression bonding
- Looking for improvements and new features on III-V chips:
  - Cleavage accuracy improvement or etched facets
  - Mechanical alignment features and spot-size convertors



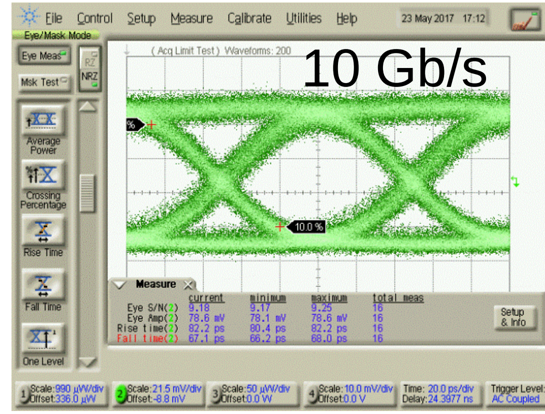
EAMs bonded on test mounts



RAPIDO

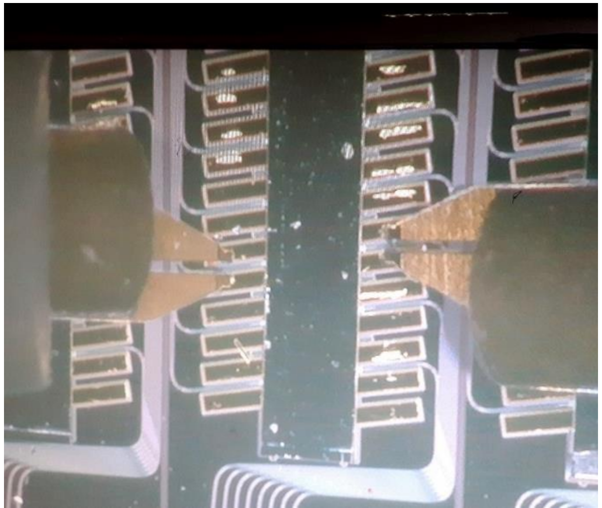
Charaterization of EAM test assemblies

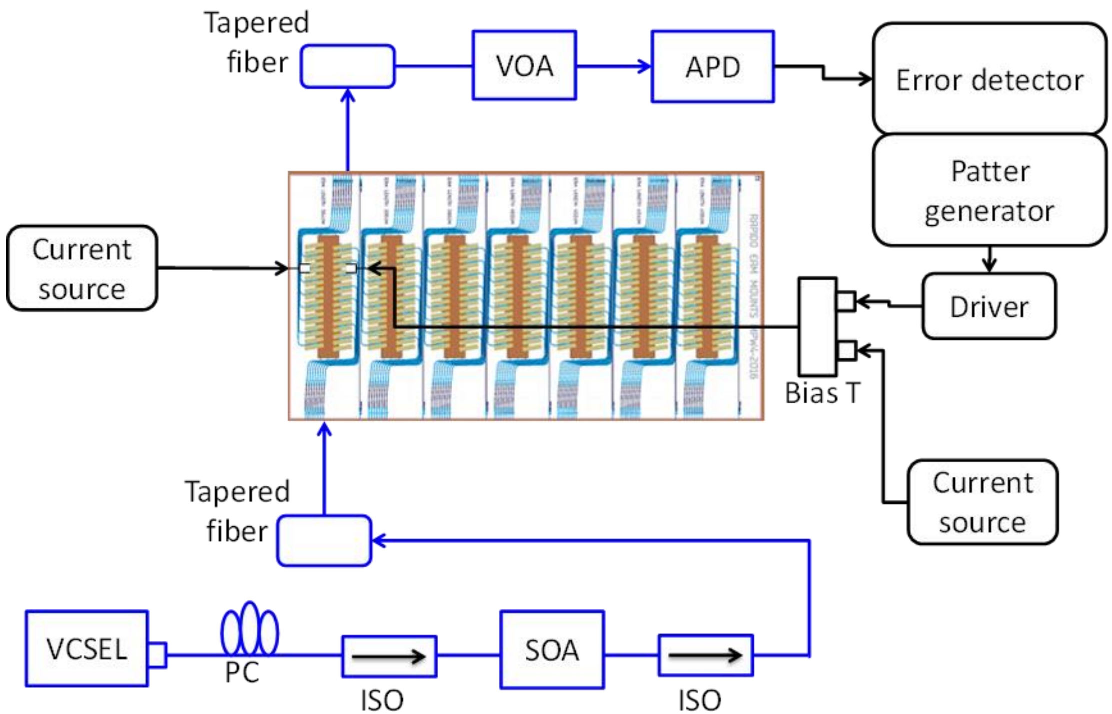
- EAM bandwidth limited by EAM design to ~10 Gb/s, which was confirmed experimentally
- Higher bandwidth up to ~40 Gb/s is possible with EAM redesign



RAPIDO

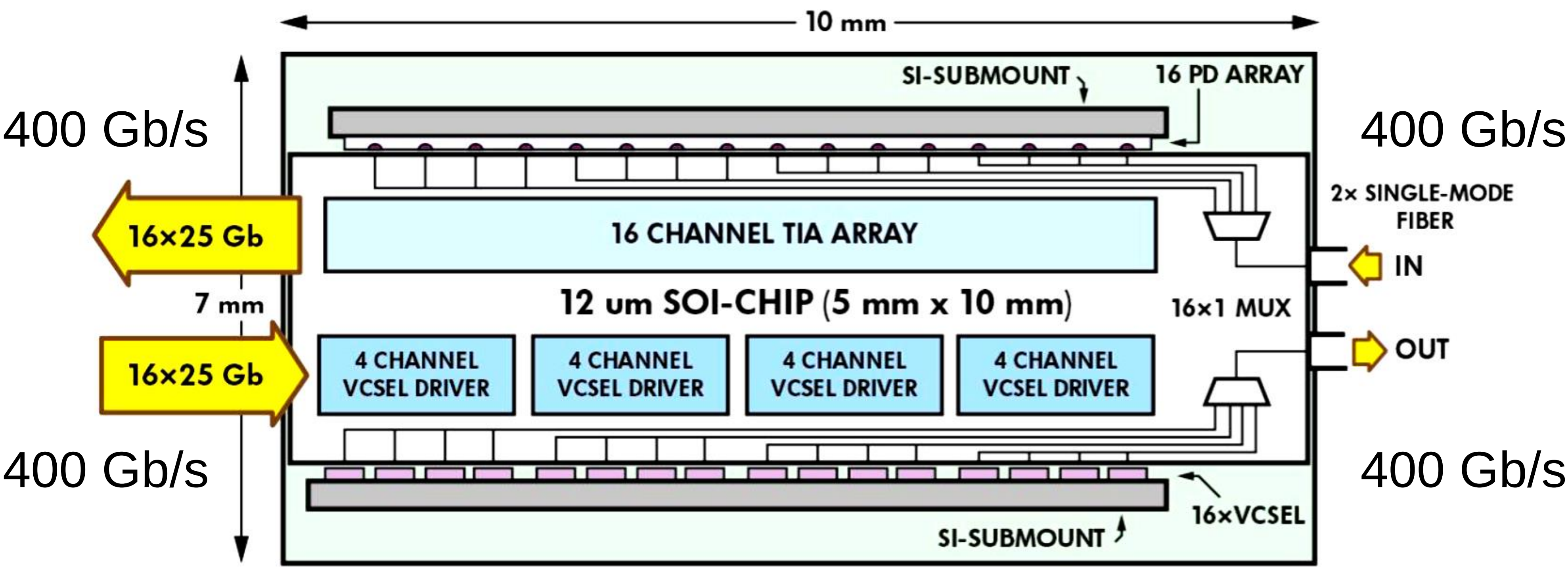
TAMPERE UNIVERSITY OF TECHNOLOGY





Simple and scalable transceivers for 400G and even beyond 1 Tb/s

Directly modulated VCSELs and discrete PD arrays:

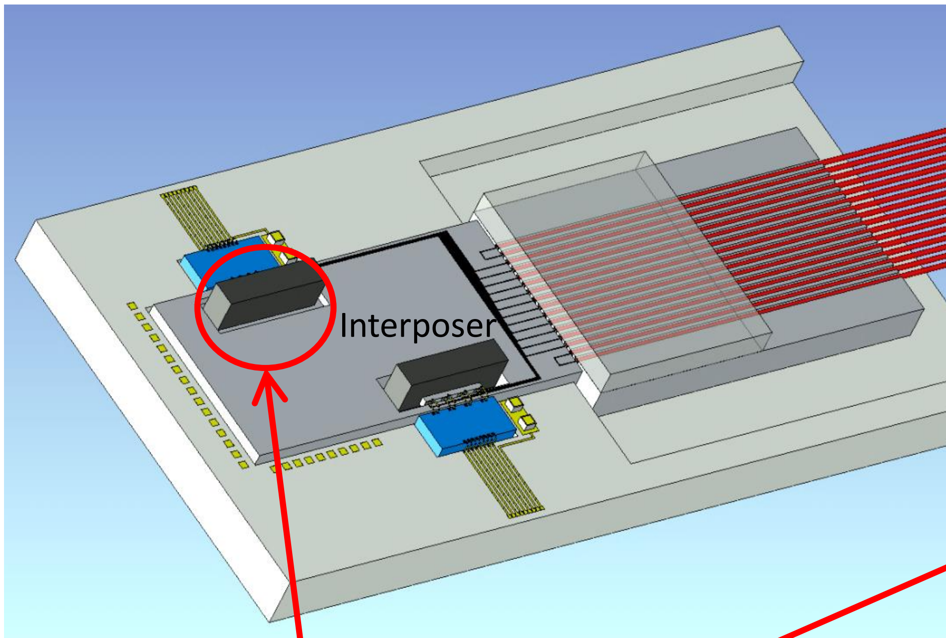


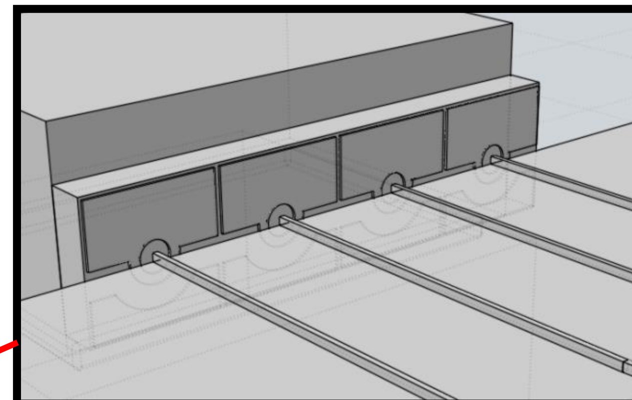
Further scaling to >>1 Tb/s with faster VCSELs, PAM-4, polarization MUX and/or more channels

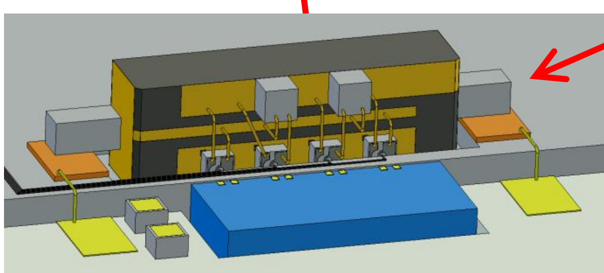
RAPIDO design for VCSEL integration on 12 µm SOI for transceivers

- VCSEL coupling to locally thinned 8 µm SOI waveguides on 12 µm SOI chip

Calculated power efficiency:
- 8.6 pJ/bit for VCSEL+driver
- 2.6 pJ/bit for PD+TIA
- Power consumption dominated by the driver





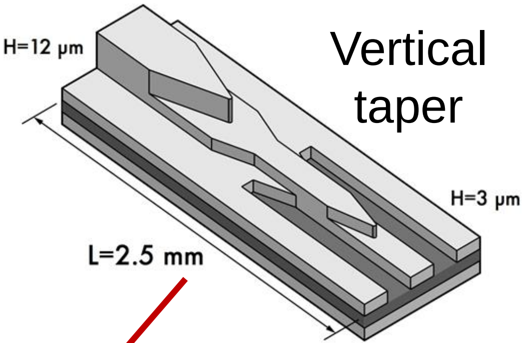


VCSEL submount assembly (with INTEC driver)

cnit
VERTILAS
imec
RAPIDO

RAPIDO transmitter demo assembly

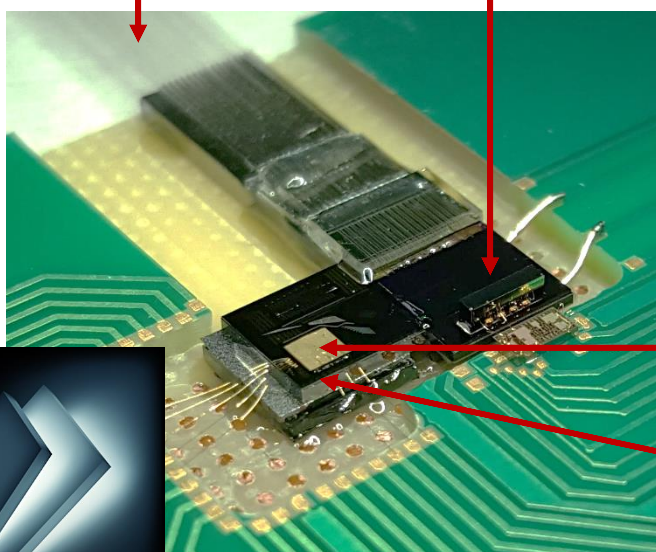
- Test assembly with VCSELs, SOAs, EAMs and drivers
- Coupling to a 3 µm SOI chip with a 12-to-3 µm taper
- Not yet functional due to high interface losses etc.

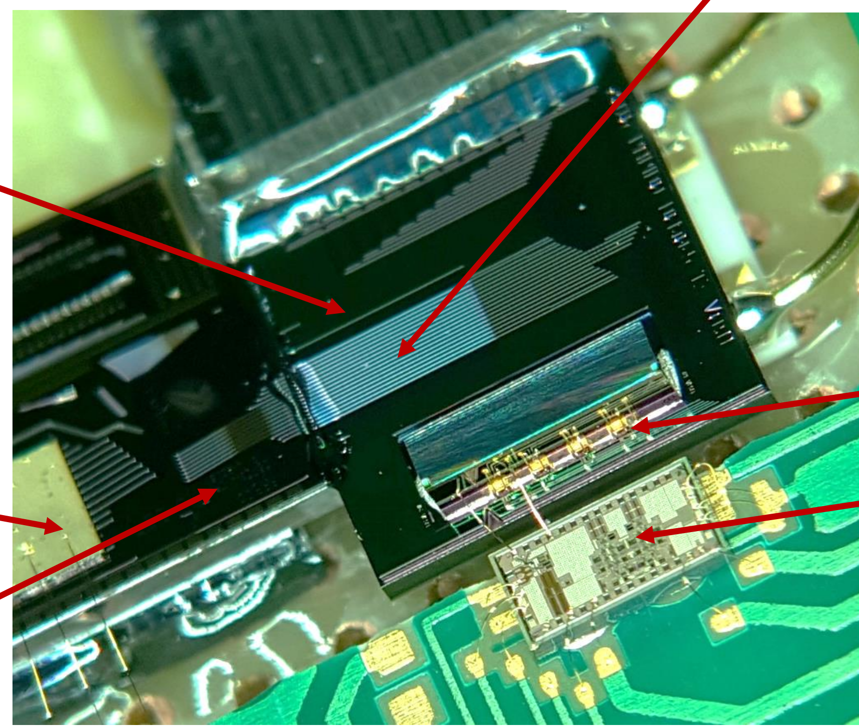


Vertical taper

Fiber array

12 µm SOI





VCSEL

Driver

SOA

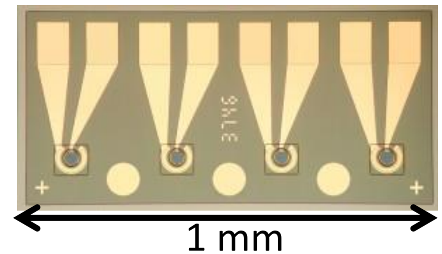
3 µm SOI

RAPIDO

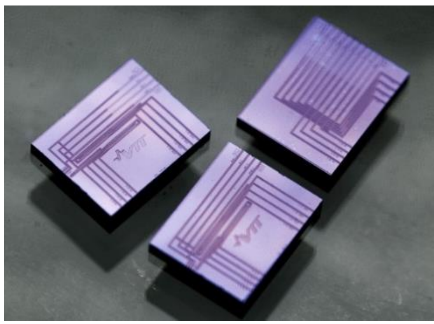
imec cnit VERTILAS TAMPERE UNIVERSITY OF TECHNOLOGY Tyndall National Institute

Revised assembly/integration plan for transceiver integration

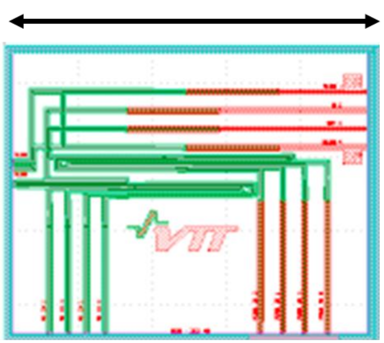
- All optoelectronics integrated on an evaluation board
- Si photonic chip with a fiber (array) is added on top.
- Uncompromised electrical performance
- Modular assembly & testing



28 Gbps PDs



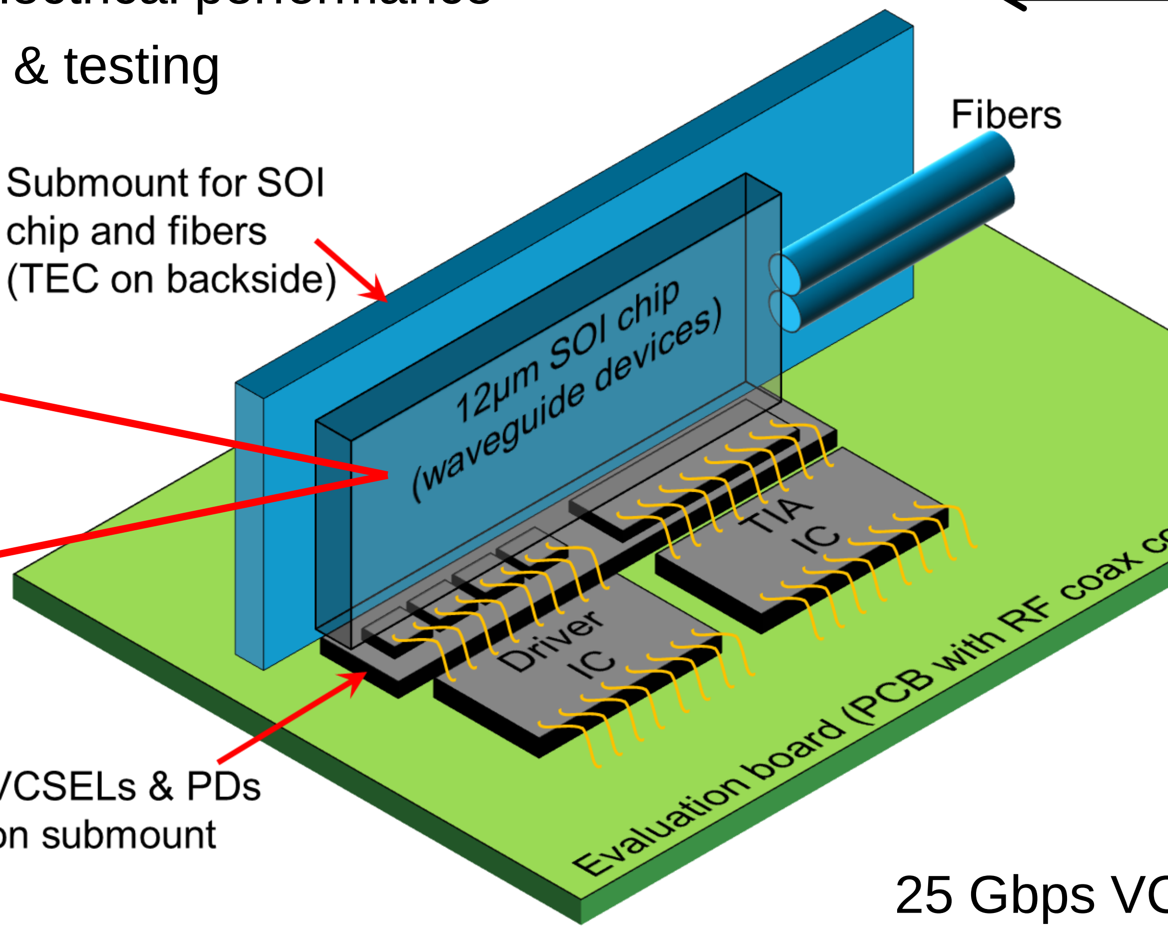
5 mm



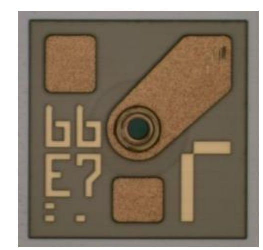
Fibers

PDs VCSELs

Submount for SOI chip and fibers (TEC on backside)



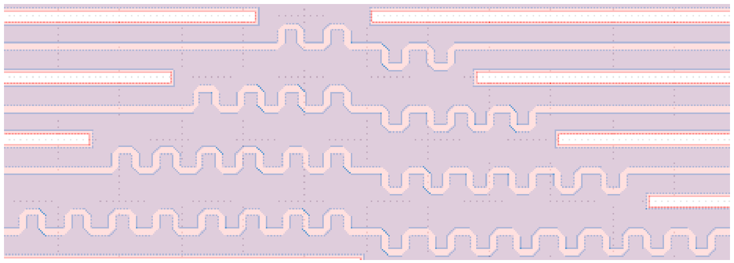
VCSELs & PDs on submount

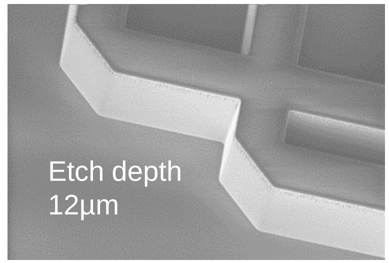


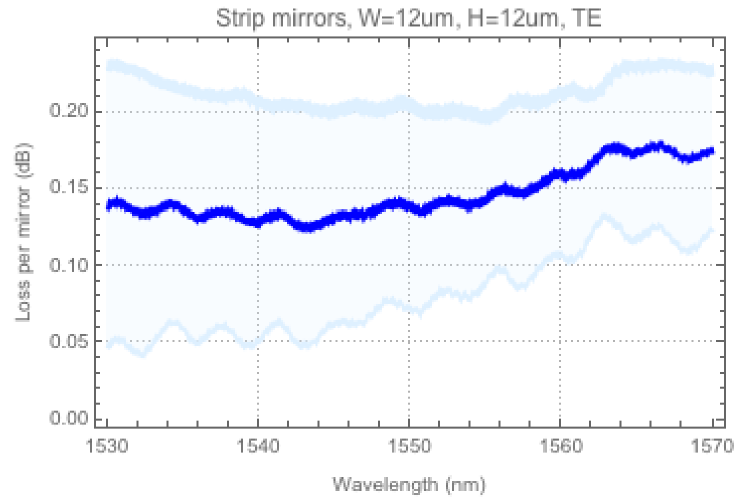
25 Gbps VCSELs

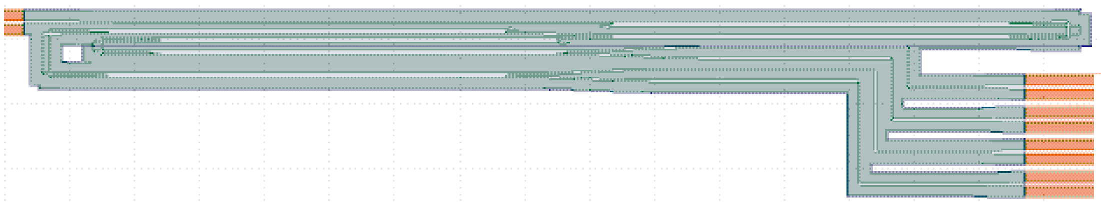
Development of mirrors and MUX/DEMUX on 12 µm SOI

- TIR mirrors demonstrated with 0.15 dB/90° loss

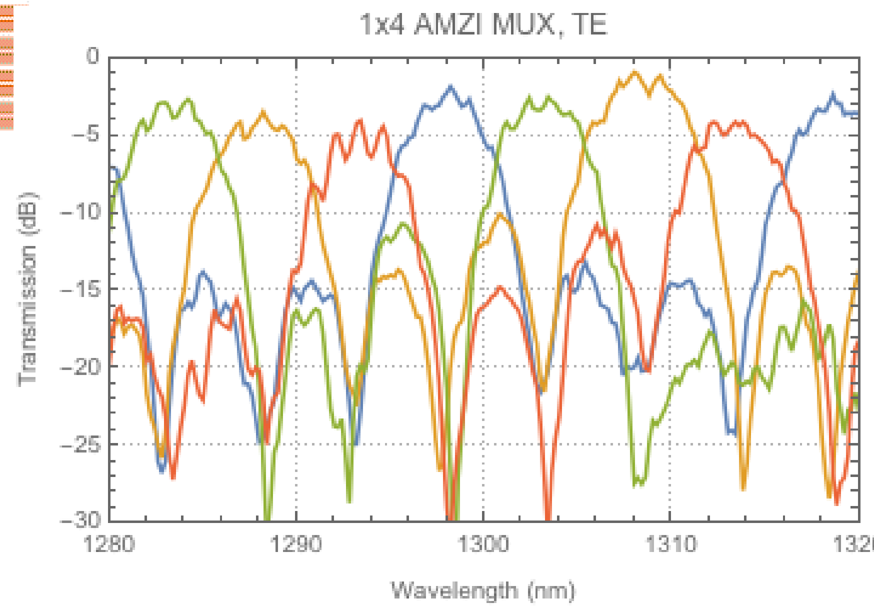






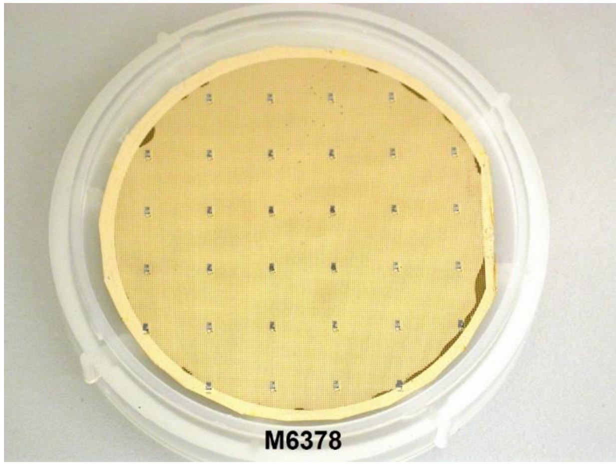


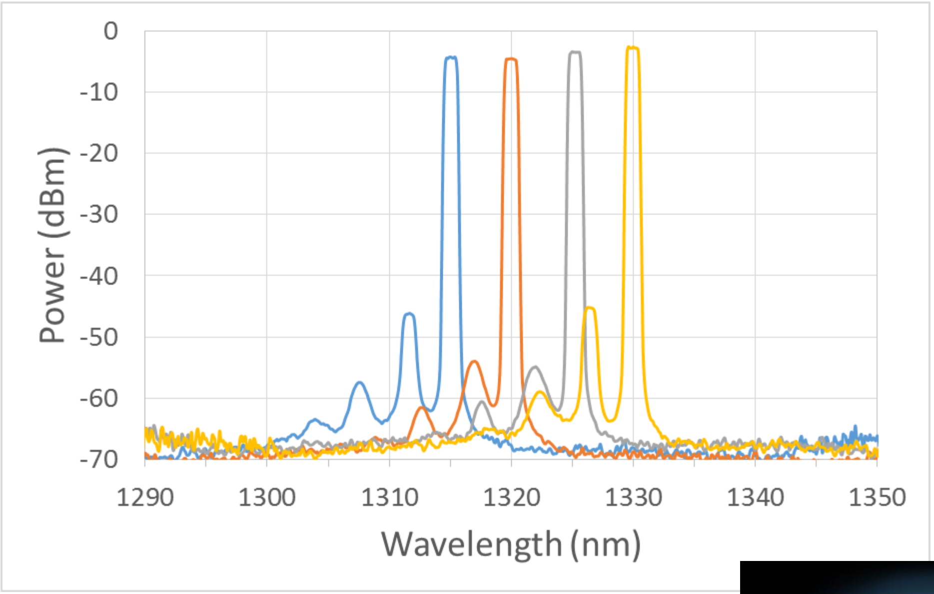
- 4x1 multiplexers with cascaded MZIs, MMI couplers and TIR mirrors with 2–5 dB loss

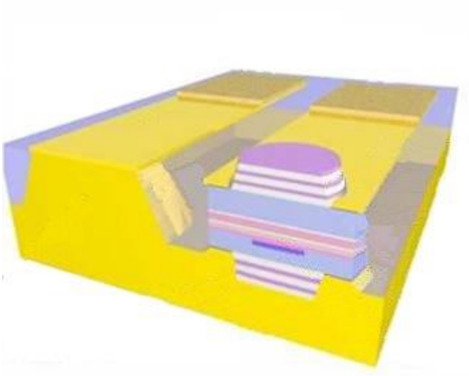


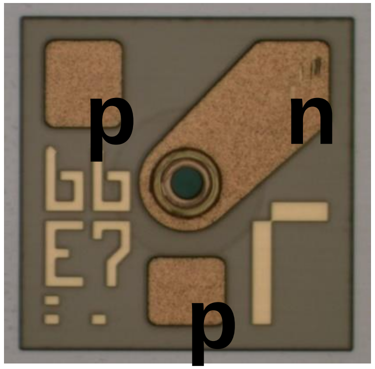
1.3 µm VCSELs with 5 nm channel spacing: Design, fabrication and testing

- New high-speed layout that supports integration on SOI
- Several wafers fabricated to cover 8 x 5 nm = 1295-1330 nm range
- ~20 000 VCSELs/wafer









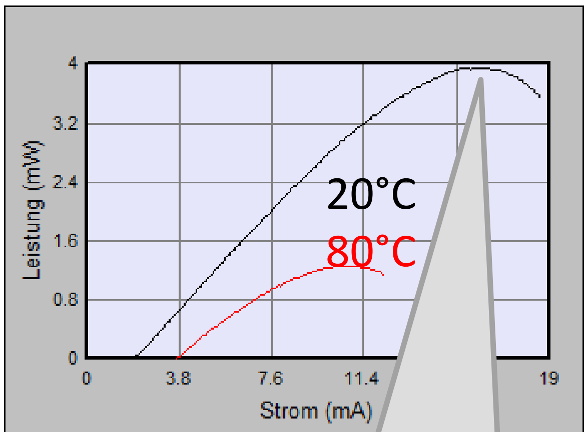
VERTILAS

RAPIDO

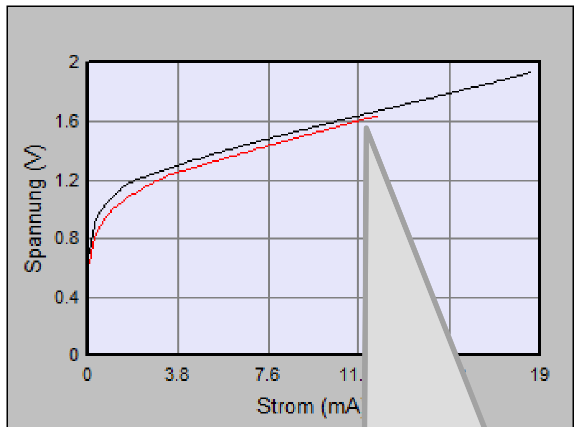
1.3 µm VCSELs with 5 nm channel spacing: Design, fabrication and testing

- VCSELs offer up to 4 mW of power with low power consumption and single-mode operation

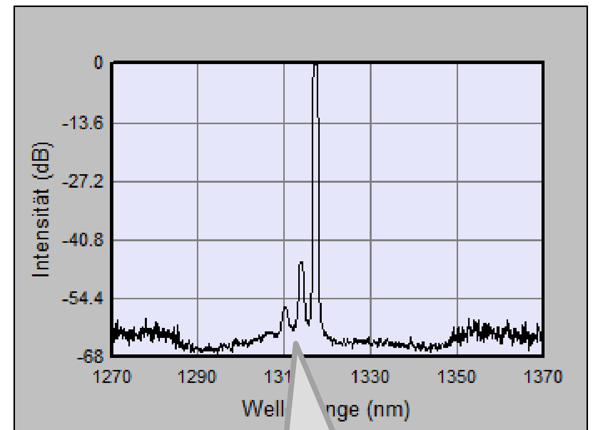
Optical Power (mW)



VI Curve



Optical Spectrum (dB)



High optical power of max. 4 mW at RT, 1.2 mW at 80°C

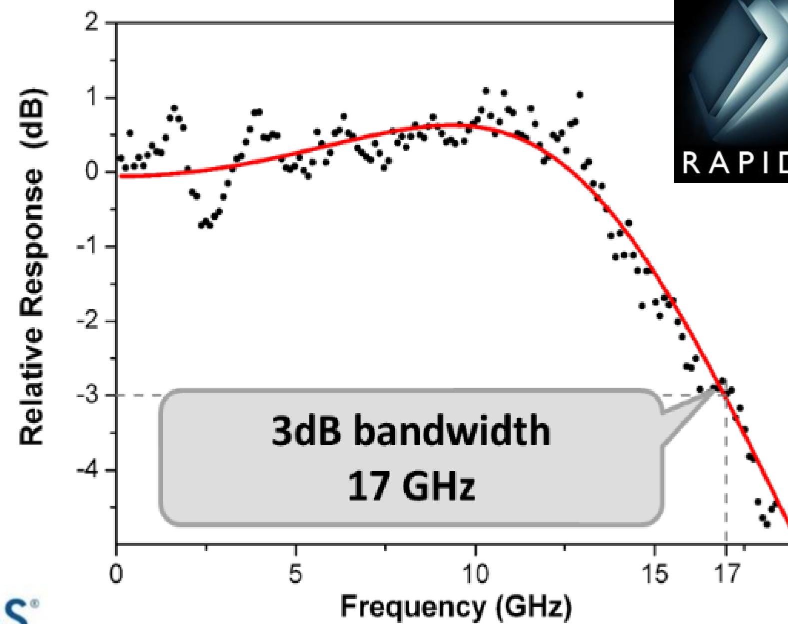
Very low power consumption 11 mA x 1.6 V < 20 mW

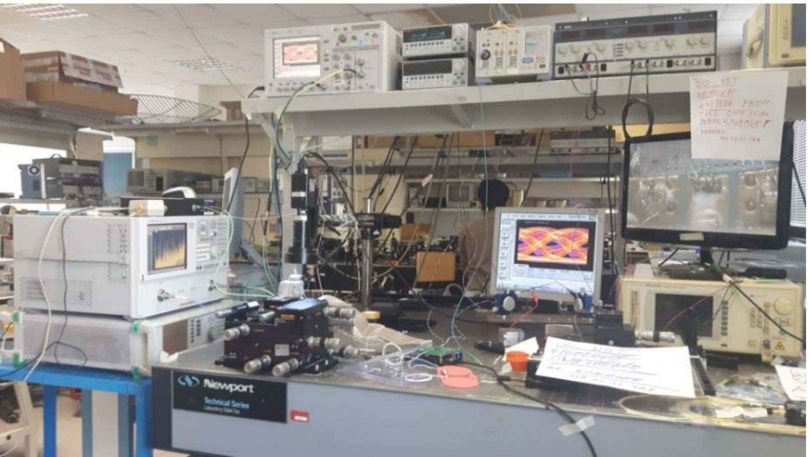
Excellent SMSR Ca. 45 dB

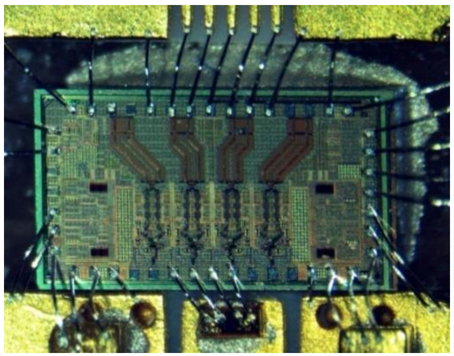
RAPIDO

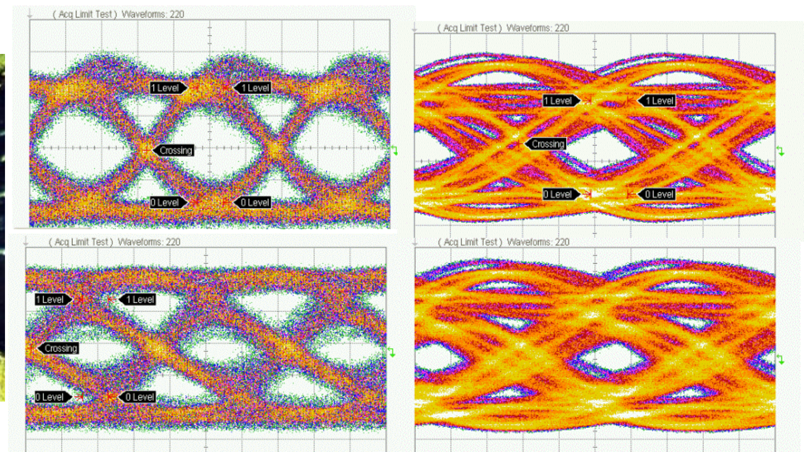
1.3 µm VCSELs with 5 nm channel spacing: Design, fabrication and testing

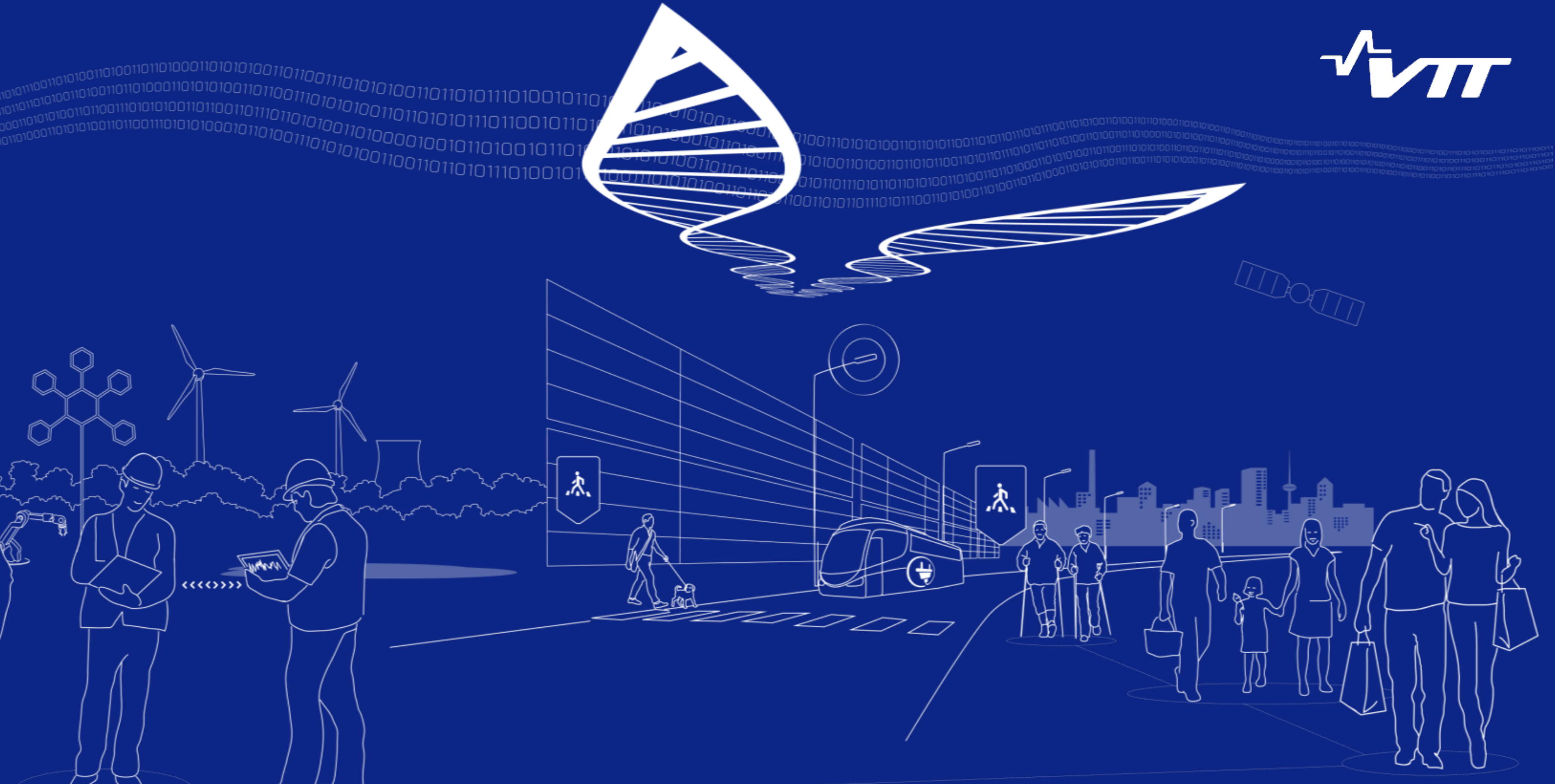
- High-speed measurements carried out up to 56 Gb/s
- For more details about high-speed VCSELs: ECOC’19 paper M.2.C.5 by Antonio Malacarne (“Low-Power 1.3-µm VCSEL Transmitter for Data Center Interconnects and Beyond”)







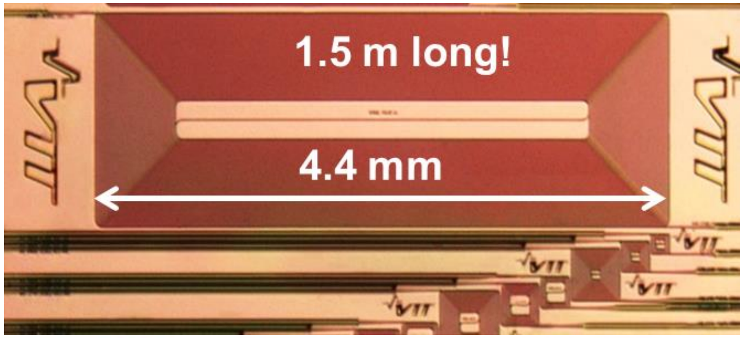


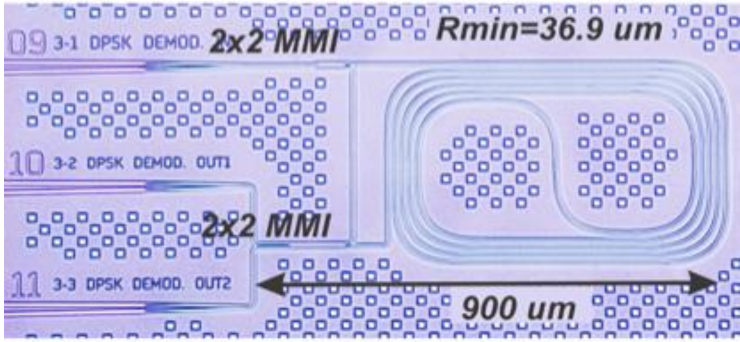


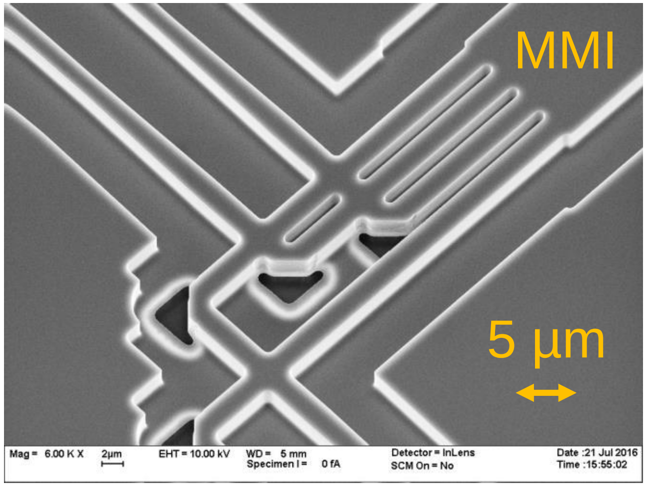
Latest advances in monolithic integration on 3 µm SOI

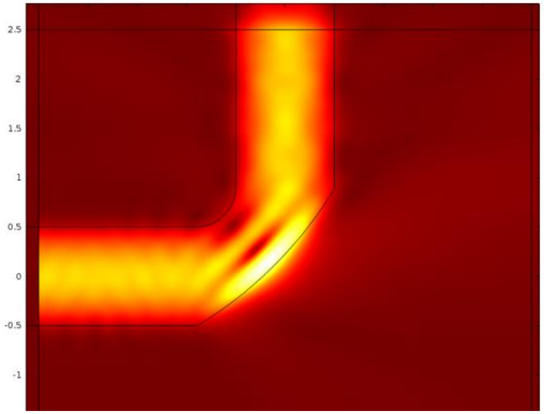
Ultra-dense spirals, delay lines and MUX based on TIR mirrors and Euler bends

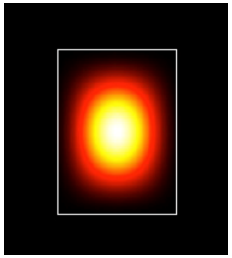
- Mirrors: ~0.1 dB/90° loss
- Euler bends: <0.01 dB/90°
- Compact spirals with low losses (0.1-0.15 dB/cm including the bends)
- Delay lines for filters, coherent receivers, microwave photonics etc.
- MZI, AWG, Echelle gratings etc.

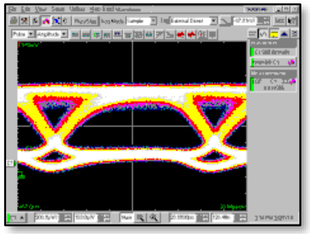










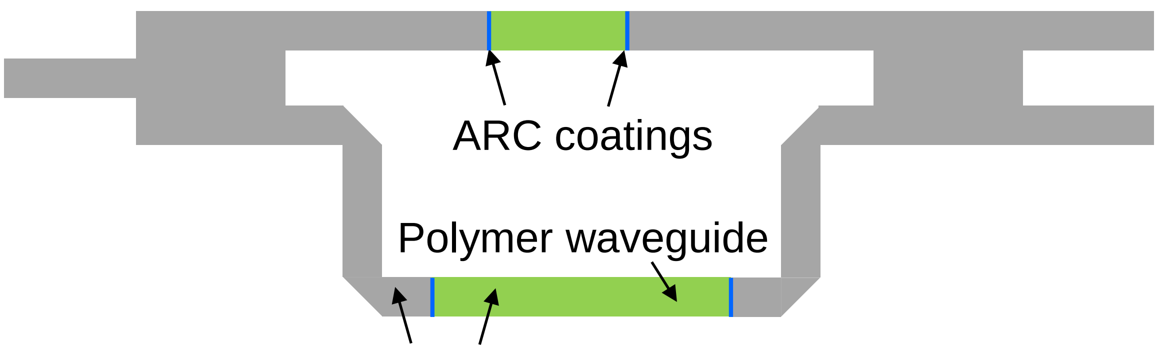


10 Gb/s DPSK demodulator

Athermal components on 3 µm SOI

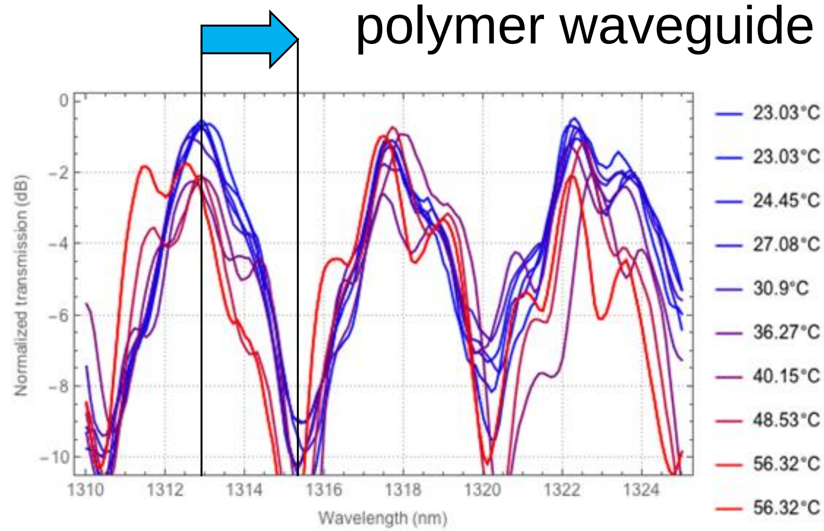
- Polymer waveguides on 3 µm SOI with opposite TO coefficient
- End-fire coupling between polymer and SOI waveguides
- First experimental results confirm athermal multiplexing/filtering
  - In SOI about 0.07 nm/K peak shift
  - In polymer-SOI multiplexer the peak shift is below the measurement resolution (~0.01 nm/K due to fiber movement during T scanning)

Mach-Zehnder interferometer:



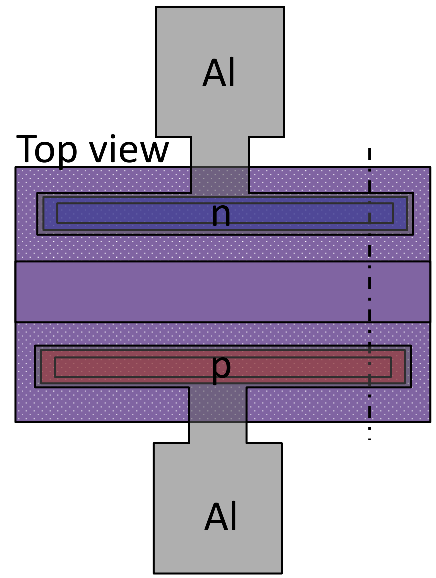
With optimized ratio of polymer and SOI waveguide lengths the temperature dependencies cancel out

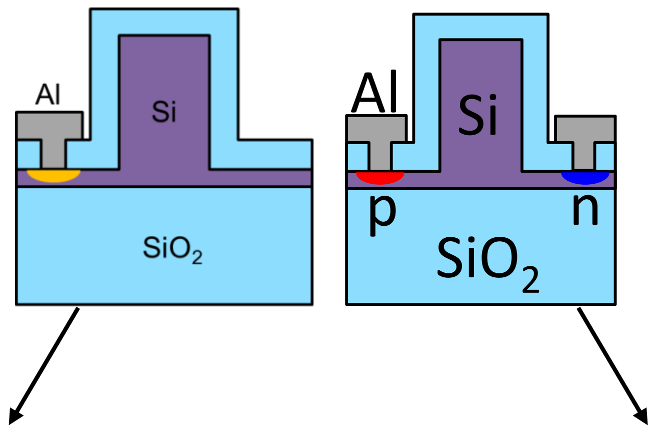
MZI peak shift with (arrow) and without polymer waveguide

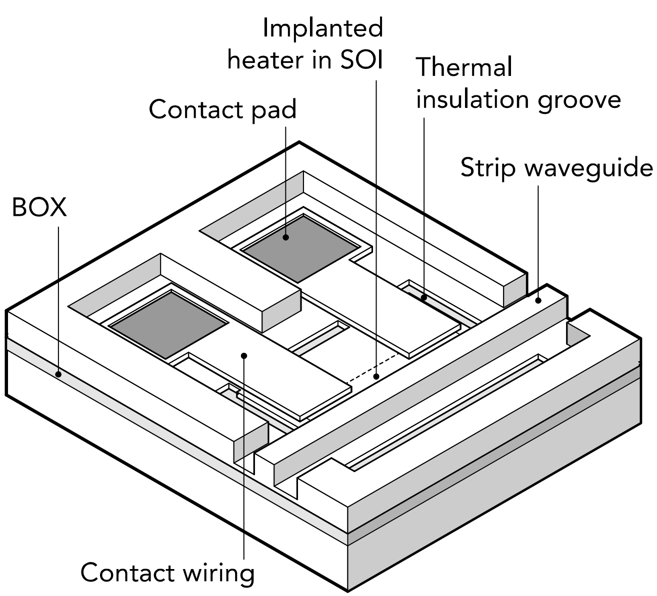


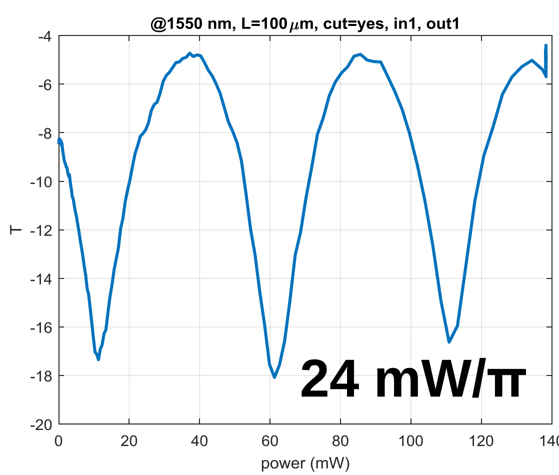
Thermo-optic and electro-optic switches

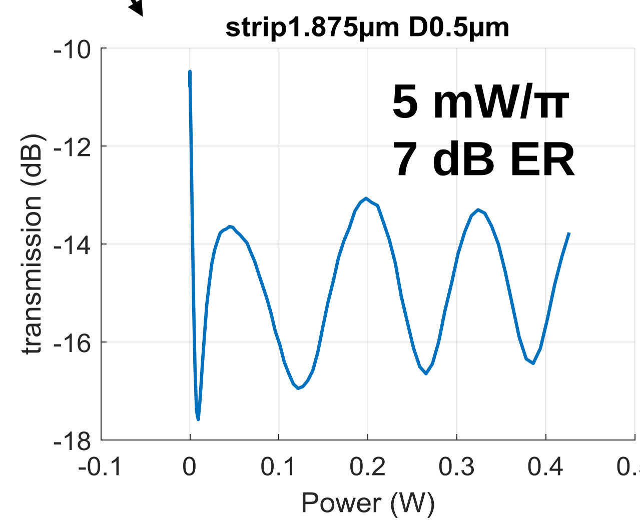
- Implanted heaters and p/n areas in a thin Si slab
- Heaters for >10 kHZ operation
- PIN modulation >1 MHz (not for data)





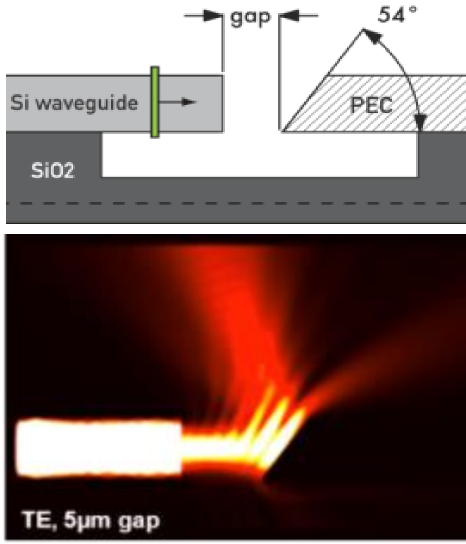


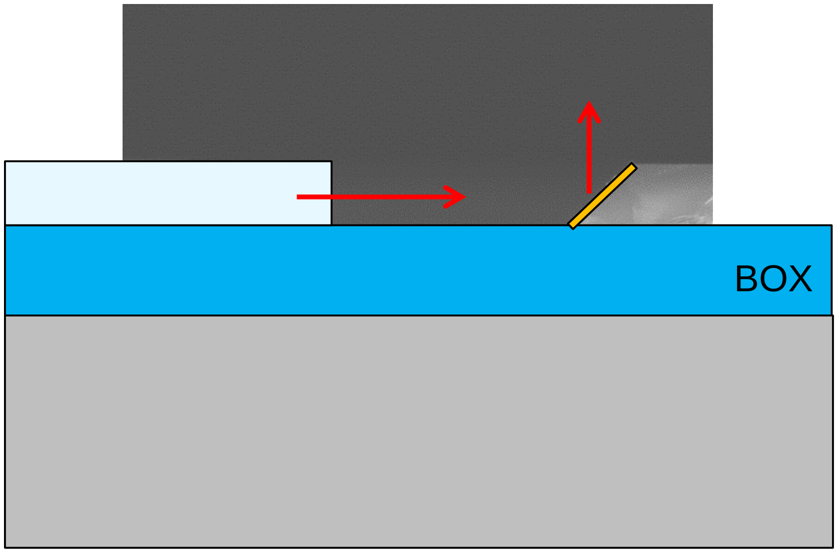


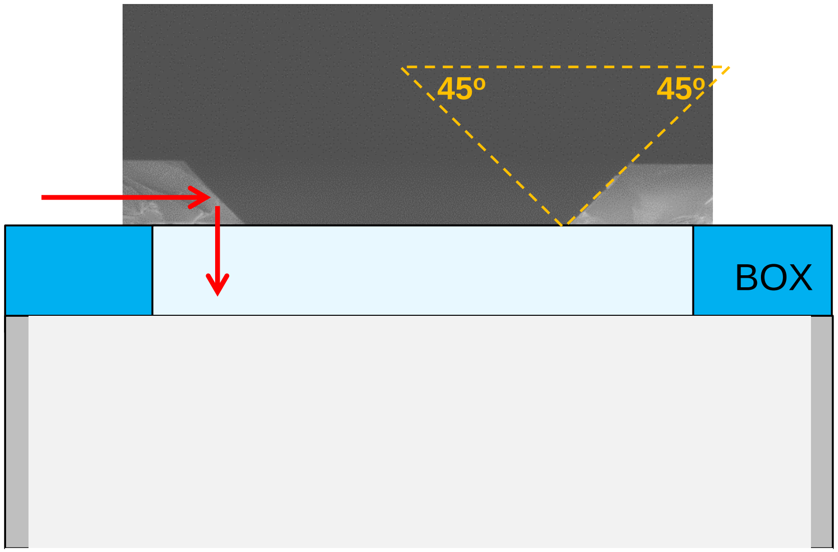


Up-reflecting mirrors for wafer level testing and VCSEL integration

- Metallized up-reflecting mirrors with 1-2 dB loss
- Output angle ~20° with standard TMAH etch
- Vertical coupling with modified etch (45° mirror)
- Reflection up (metal mirror) or down (TIR)

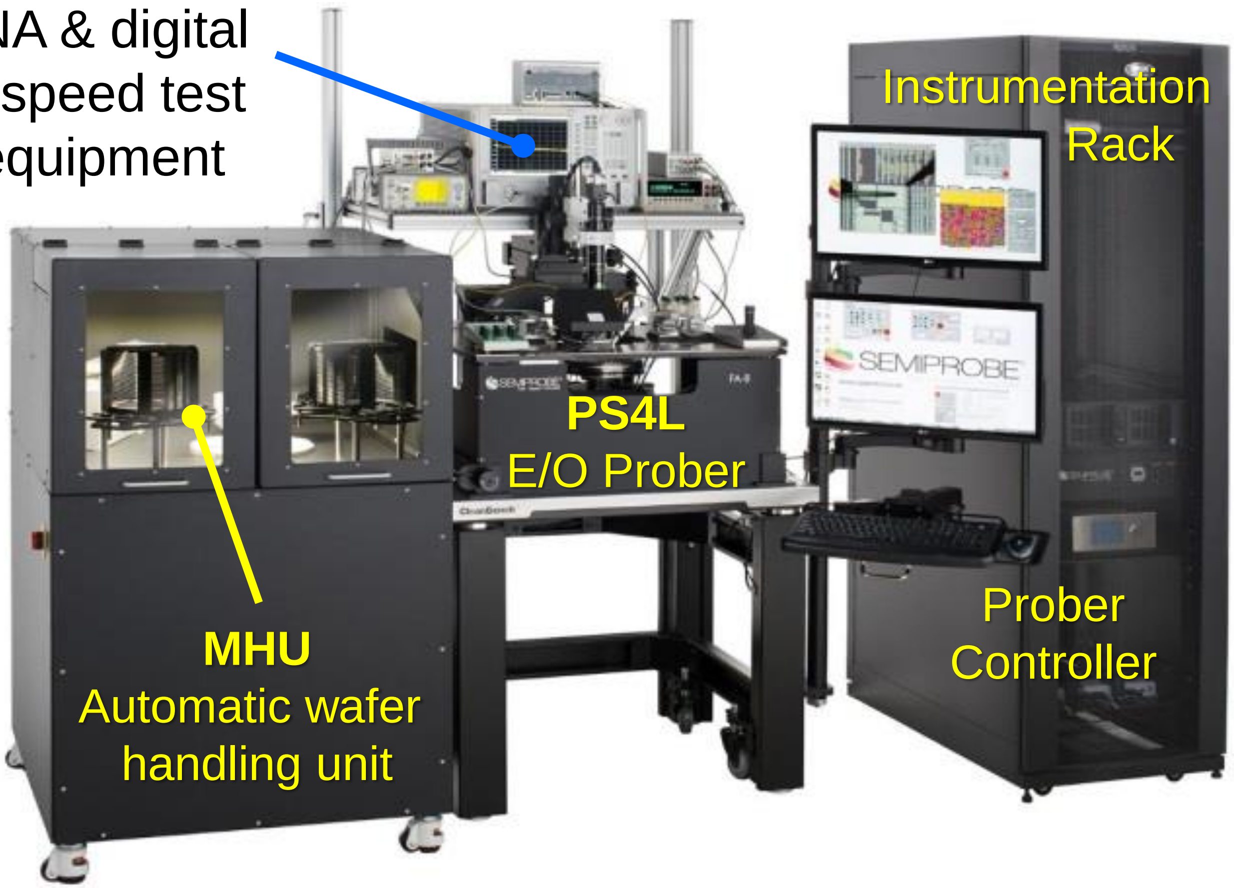


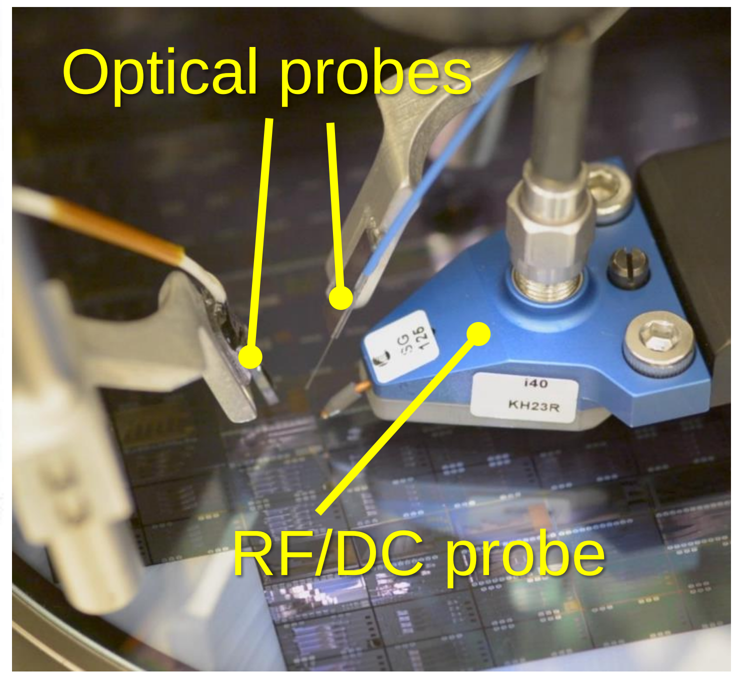


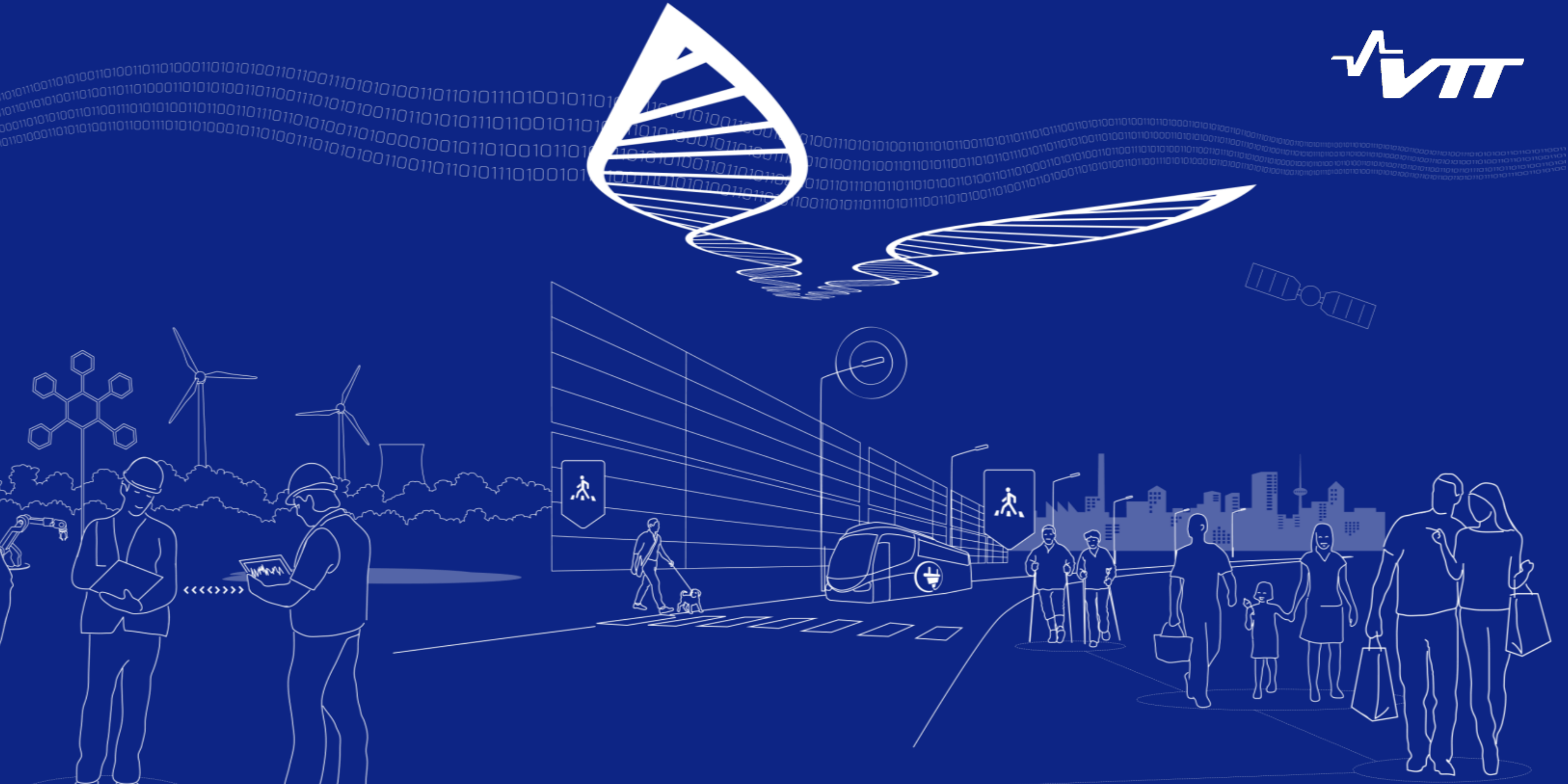


Automated wafer level testing to ramp up production and to speed up R&D

- Simultaneous electrical & optical probing is necessary for active devices
- Full automation is necessary to ramp up production (cassette-to-cassette)







Faraday rotation in 3 µm SOI waveguides

Faraday rotation in Thick SOI

- Collaboration with Hamburg University of Technology
- Chips provided to TUHH from VTT's standard MPW runs
- Promising path towards a low-loss and broadband isolator on a chip
- Poster in Group Four Photonics (GFP) 2017:

TUHH Hamburg University of Technology

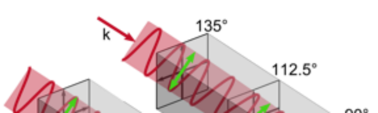
Faraday rotation in silicon waveguides

Dirk Jalas,[1,*] Nabeel Hakemi,[1] Matteo Cherchi,[2] Mikko Harjanne,[2] Alexander Yu. Petrov,[1,3] and Manfred Eich[1,4]

[1]Institute of Optical and Electronic Materials, Hamburg University of Technology, Eissendorfer Strasse 38, 21073 Hamburg, Germany
[2] VTT Technical Research Centre of Finland, Espoo, 02040, Finland
[3]ITMO University, 49 Kronverkskii Ave., 197101, St. Petersburg, Russia
[4]Institute of Materials Research, Helmholtz-Zentrum Geesthacht, Max-Planck-Strasse 1, 21502 Geesthacht, Germany
*email : dirk.jalas@tuhh.de

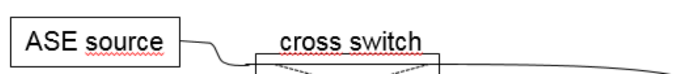
We propose a novel concept for a Faraday rotator which utilizes silicon as a sole magneto-optical active material. Although, silicon has a Faraday rotation two orders of magnitude smaller than commonly used materials, its extremely low losses in the NIR allow for long device lengths. To keep the footprint small, we present a concept for wrapping up the Faraday rotator in a spiral fashion. 180° phase shifters are proposed to allow continuous accumulation of the Faraday rotation in a folded waveguide.

The problem of bending a Faraday rotator



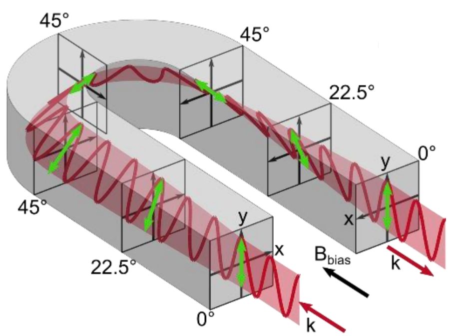
A Faraday rotator rotates linear polarized light by a certain degree. The

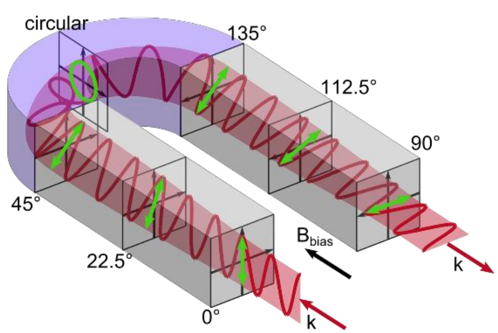
Proof of concept



Faraday rotation in Thick SOI

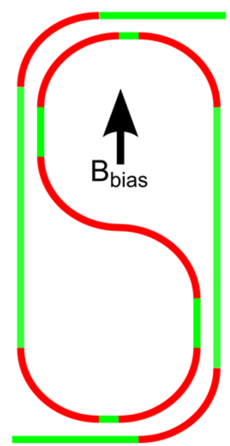
- Silicon used as a magneto-optical active material
- Faraday rotation is x100 smaller in Si than in commonly used materials, but sufficient in a long, low-loss and polarization independent waveguide
- 180° phase shift in bends to achieve continuous Faraday rotation
- Polarization rotation in Si is ~15°/K/cm and 0.5T was used to achieve 4 dB extinction ratio in the first demonstration



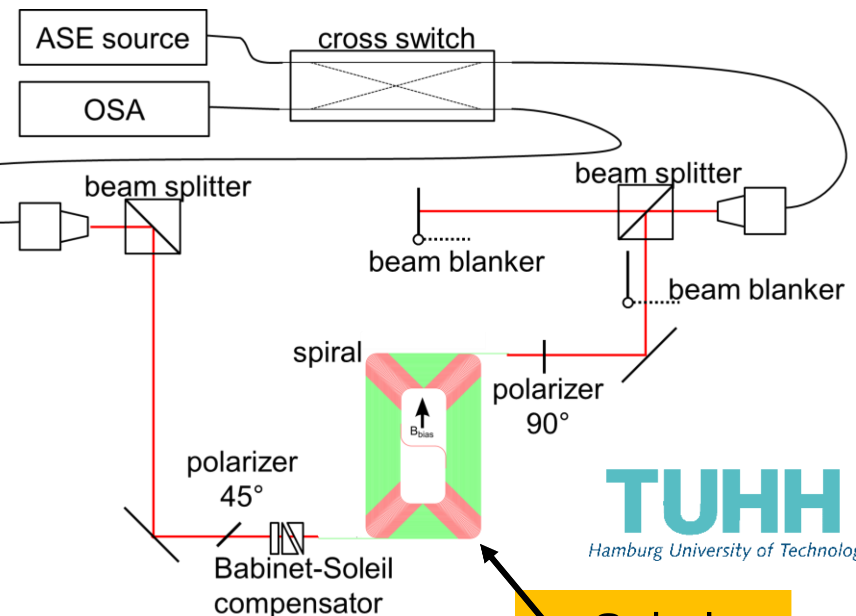


Polarization rotation cancels out in a conventional layout

…but can accumulate if birefringent bends reflect polarization



← 6 cm long



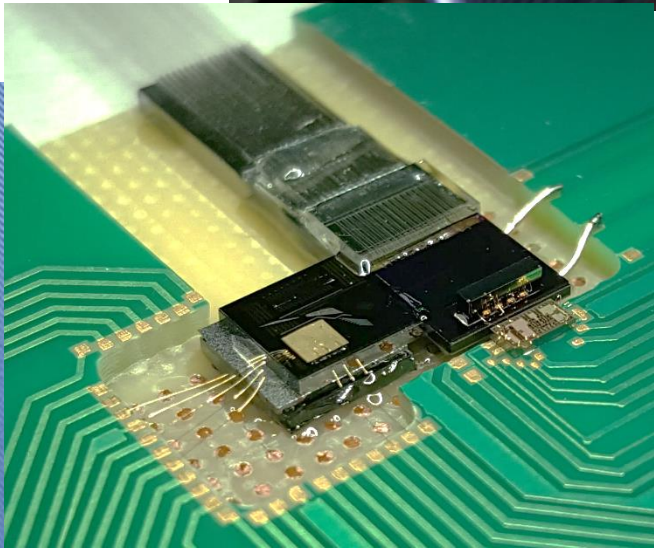
Spiral footprint ~0.5 mm²

TUHH
Hamburg University of Technology

Conclusions & Outlook

Conclusions

- Hybrid integration of Thick-SOI and III-V offers a versatile platform for optical interconnects and other applications
- Directly modulated long-wavelength VCSELs match well with micron-scale SOI waveguides
- Thick-SOI technology offers low loss PICs with SM, athermal and polarization independent operation
- On-going development for isolator, 400G transceiver and monolithically integrated (fast) PDs and modulators
- R&D and small/medium volume manufacturing offered by VTT and VTT Memsfab Ltd.



Acknowledgments

- We thank EU, Tekes and industrial partners for funding and all R&D partners for fruitful collaboration
- RAPIDO-project (EU FP7, grant agreement 619806)
- OPEC-project (TEKES)

PROJECTS

PARTNERS

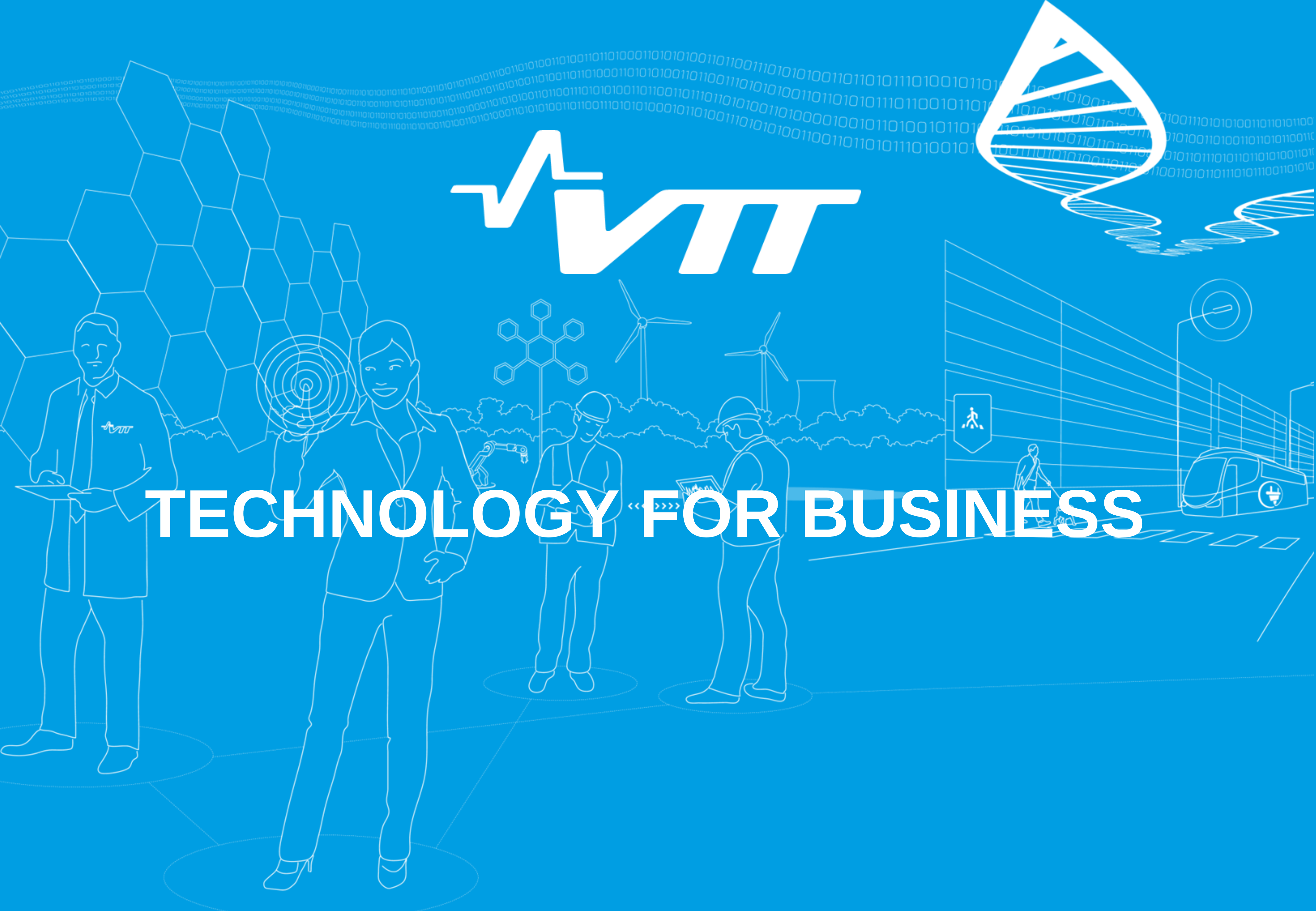
NETWORKS & FUNDING

Contact and information:

silicon.photonics@vtt.fi

www.vtt.fi/siliconphotonics

www.rapido-project.eu


TECHNOLOGY FOR BUSINESS