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L3MATRIX – large, low power and low cost data centers

Concurrently, disaggregation and virtualization trends in the DC are forcing the traffic to be between servers and storage elements in the east-west direction. These changes require massive switching capabilities from the discrete switch elements. However, the technology is rapidly reaching a limit. The result is a multi-layered DC topology with high power consumption and long latency. The L3MATRIX project provides novel technological innovations in the fields of silicon photonics (SiP) and 3D device integration. The project will develop a novel SiP matrix with a scale larger than any similar device with more than 100 modulators on a single chip and will integrate embedded laser sources with a logic chip thus breaking the limitations on the bandwidth-distance product.

A novel approach will be used with embedded III-V sources on the SOI substrate which will eliminate the need to use an external light source for the modulators.

L3MATRIX provides a new method of building switching elements that are both high radix and have an extended bandwidth of 25 Gb/s in single mode fibres and waveguides with low latency. The power consumption of DC networks built with these devices is 10-fold lower compared to the conventional technology. The outcome of this approach is that large networks, in the Pb/s scale can be built as a single stage, non-blocking network.

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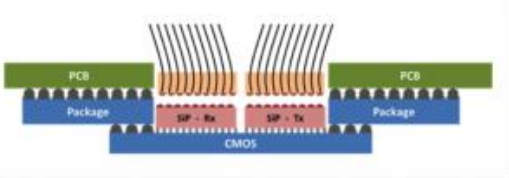

Objectives, potential technology breakthroughs, specific innovation challenges and potential market barriers:

- Scaling of the network to provide a solution to the growing demands for bandwidth.
- Increasing the reach of the optical interconnects within the site given its size and the need to connect servers directly in the east-west direction
- Minimizing the port-to-port latency to enable timing-critical processes such as disaggregated memory access or cache-coherent systems.
- Cost reduction, primarily in electrical power consumption and total cost of ownership.
- Two-dimensional Silicon Photonics chip with 128 lanes on 100mm2 requiring a density of ~0.8mm2 per channel including integrated hybrid silicon III-V laser sources
- Improvement of the power efficiency to the 3pJ/bit range
- Reduce the port-to-port latency to less than 20ns
- Scalable data centre architecture into the Pb/s scale

Partners:

- FRAUNHOFER IZM | Germany
- DUST Photonics | Israel
- AMS AG | Austria
- IBM RESEARCH GMBH | Switzerland
- ARISTOTELIO PANEPISTIMIO THESSALONIKIS | Greece
- UNIVERSITAT POLITECNICA DE VALENCIA | Spain
- BRIGHT PHOTONICS BV | Netherlands
- UNIVERSITY COLLEGE LONDON | United Kingdom